

Edited by Bill Travis

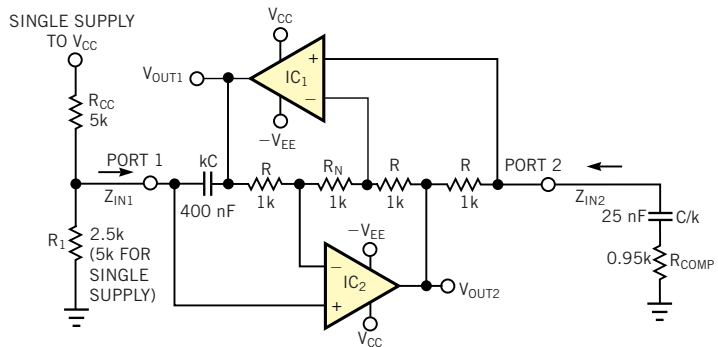
GIC resonator has inherent amplitude control

Lutz von Wangenheim, University of Applied Sciences, Bremen, Germany

THE CIRCUIT IN **Figure 1** is based on a classic GIC (generalized impedance converter). The sine-wave-oscillator circuit has inherent amplitude stabilization and normally operates from dual power supplies. However, if you connect an additional resistor, R_{CC} , to V_{CC} , you can operate the circuit with one supply (with $V_{EE} = 0V$). You can adjust the oscillation frequency by varying R_1 . R_{COMP} ensures oscillation and does not affect the oscillation frequency. The remaining passive components are four equal-value resistors, R , and two capacitors, kC and C/k , where k is a scaling factor. This modification of the classic GIC structure incorporates an additional resistor, R_N , between both inverting op-amp inputs. The GIC topology has excellent high-frequency properties and thus finds extensive use in active-filter circuits. The GIC structure can simulate a grounded inductance or a grounded FDNR (frequency-dependent negative resistance).

You can explain the function of the circuit by starting with the GIC input impedance at either Port 1 or Port 2. A straightforward analysis of the circuit yields the input impedance at Port 1:

Figure 1



A GIC-based resonator provides inherent amplitude control and low distortion.

$$Z_{IN1} = -\frac{1}{\omega^2 C^2 R} - \frac{1}{j\omega kC} \left(\frac{R_N}{R} - \frac{R_{COMP}}{R} \right).$$

$$f_0 = \frac{1}{2\pi C \sqrt{RR_0}}.$$

Note that, for $R_{COMP} = R_N$, the expression for Z_{IN1} represents the input impedance of an ideal FDNR. The FDNR, together with an ohmic shunt resistance from Port 1 to ground, forms a tuned circuit with the inherent capability to oscillate. In reality, however, the oscillation would die out because of parasitics arising from lossy capacitors and imperfect amplifiers. The circuit in **Figure 1** compensates for these losses by using the second portion of Z_{IN1} , representing a negative capacitance for $R_{COMP} < R_N$. In practice, you should choose $R_N = R$ and a resistor ratio, R_{COMP}/R , close to unity (for example, $R_{COMP}/R = 0.95$ to 0.98). If you perform the analysis at Port 2 of the circuit, the input impedance, Z_{IN2} , represents an ideal inductance in series with a negative resistor. Shunting this impedance with a capacitor-resistor branch (C/k and R_{COMP} in **Figure 1**) creates a lossless LC tank circuit. This tank circuit can oscillate if you satisfy the condition $R_{COMP} < R$. The circuit starts reliably and oscillates at the following frequency:

For the circuit values in **Figure 1**, IC_2 saturates, providing a clipped sinusoidal signal at V_{OUT2} . V_{OUT1} is a filtered version of that signal. Thus, no extra circuitry is necessary for amplitude stabilization. However, the quality of the sinusoidal signal at V_{OUT1} depends on the Q factor of the resonator circuit, as the following equation states:

$$Q = \frac{k \cdot \sqrt{RR_0}}{R_N - R_{COMP}}.$$

For the values shown, a quality factor $Q > 100$ results with a capacitance scaling factor $k = 4$, $C = 100$ nF, and $(R_N - R_{COMP}) = 50\Omega$. V_{OUT1} provides a signal with a total harmonic distortion lower than 1% at $f_0 = 1$ kHz. The peak-to-peak amplitude of the sinusoidal signal is approximately 1V lower than the total supply-voltage span.

Is this the best Design Idea in this issue? Select at www.edn.com.

GIC resonator has inherent amplitude control.....**89**

Three parts provide tenfold increase in switcher current.....**90**

IC maintains uniform bias for GaAs MESFETs.....**92**

Add gain to an absolute-value amplifier**94**

Use a PIC for automatic baud-rate detection**96**

Design low-duty-cycle timer circuits.....**98**

Publish your Design Idea in EDN. See the What's Up section at www.edn.com.

Three parts provide tenfold increase in switcher current

Wayne Rewinkel, National Semiconductor, Sunnyvale, CA

INDUSTRIAL-CONTROL CIRCUITS often derive their power from widely varying sources that can exceed the 40V maximum rating of popular switching ICs. This Design Idea presents a simple, flexible, and inexpensive buck switcher that converts an input voltage as high as 60V to 5V at several amps. The circuit is unique in that it boosts current with almost no compromise in performance, size, or cost. It should be of interest to anyone who has ever searched for a simple step-down switcher with an output current or input voltage exceeding that of off-the-shelf devices. Such a search usually entails a far more complex and costly solution than the one this Design Idea presents. National Semiconductor's (www.national.com) LM2594HV and LM2597HV both feature 60V maximum input, 150-kHz operation, 0.7A peak output, and on/off capability. The 2597 adds soft start, delay, a power-good flag, and a pin you can use to bootstrap most of its bias current from V_{OUT} . Although both devices are single-chip switchers, you can also use them as driver-controllers with only slight modifications to their standard buck-regulator circuit configurations. **Figure 1** shows the 2597HVM in a typical 5V, 0.5A configuration that uses all the IC's features. **Figure 2** shows the

higher current configuration with only three additional components to boost output current to more than 6A.

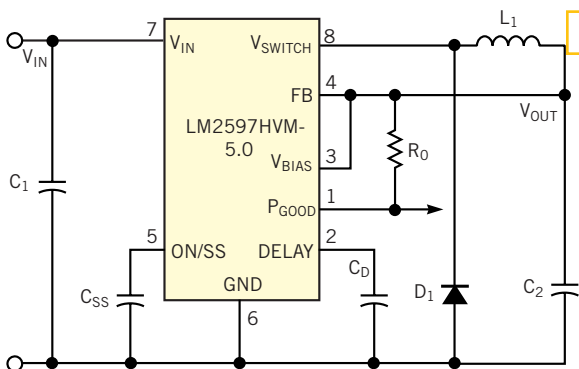
As a bonus, the circuit in **Figure 2** also provides overcurrent and short-circuit protection for Q_1 . The rugged self-protection features of the IC also apply to Q_1 , provided that the transistor has sufficient heat sinking; L_1 stays out of saturation if you select R_1 properly. If the peak current in R_1 produces a voltage drop large enough to cause Q_1 to saturate, then the IC experiences an overcurrent condition, causing its internal protection modes either to disable the switch for the remainder of the pulse period or to skip pulses. Q_1 needs to be a fast switch to minimize switching losses. The transistor also needs to have minimal storage time to avoid pulse skipping at low duty cycles. **Table 1** shows circuit performance at its maximum input voltage, 60V, under a variety of output conditions. The **table** also includes component values and ratings necessary to select sources for L_1 , C_1 , and C_2 .

Efficiency for test conditions of $V_{IN} = 60V$ and $I_{OUT} = 2$ to 6A measures 77% for $V_{OUT} = 5V$ and rises to 87% for $V_{OUT} = 12V$. Efficiency is highest for the V_{IN} range of 30 to 40V, where its peak is 2% higher than the values in **Table 1**.

Power dissipation is almost evenly divided among L_1 , D_1 , and Q_1 , so you should space these components to avoid hot spots and provide heat-sinking for as much as 3W each at maximum current and voltage. A good layout should include lots of ground plane and short, wide traces on high-current paths. Output voltages other than 3.3, 5, and 12V are also available by substituting the adjustable version of the 2597. This IC requires an added resistor pair from V_{OUT} to the FB pin to ground. Calculate resistor-divider values to set the FB pin at 1.23V for the desired output voltage. Although this design example uses the LM2597HVM-5.0, you can easily apply this current-boost technique using only three additional parts to any of National's second-generation buck devices, effectively extending their output-current capability more than tenfold. You need not use HV devices for applications with a maximum input voltage lower than 40V. The following seven steps provide a simplified procedure to select component values for a wide range of operating conditions, including those that **Table 1** lists:

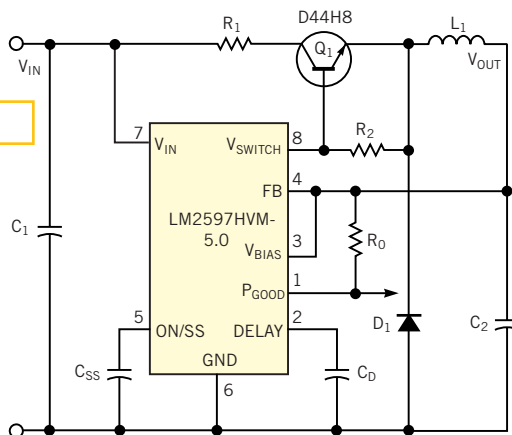
1. Choose R_1 to drop 1.5V at the inductor's peak operating current of $I_{OUT} + 20\%$. A higher current peak can

Figure 1



This classic buck-regulator circuit efficiently steps down voltage.

Figure 2



You can increase output current more than tenfold with the addition of only three components.

TABLE 1—EFFICIENCY VERSUS OUTPUT VOLTAGE AND CURRENT

Efficiency (%)	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (A)	R ₁ (Ω)	R ₁ (W)	R ₂ (Ω)	Q ₁ D4448	D ₁ (V at A)	L ₁ (μH)	L ₁ ESR (Ω)	L ₁ LSAT (A)	C ₁ (μF)	C ₁ ESR (Ω)	C ₂ RMS (A)	C ₂ (μF)	C ₂ ESR (Ω)	C ₂ RMS (A)
77	60	5	1	1	0.06	4.7	D4448	60/1	68	0.13	1.2	100	0.22	0.5	100	0.22	0.12
78	60	5	2	0.5	0.15	4.7	D4448	60/3	47	0.086	2.4	220	0.11	1	220	0.11	0.2
77	60	5	4	0.33	0.5	4.7	D4448	60/6	34=68×2	0.065	4.8	470	0.065	1.8	470	0.065	0.3
77	60	5	6	0.22	0.7	4.7	D4448	60/6	20=10×2	0.056	7.2	680	0.047	2	680	0.047	0.6
85	60	12	1	1	0.16	4.7	D4448	60/1	150	0.25	1.2	100	0.22	0.6	100	0.22	0.11
86	60	12	2	0.5	0.42	4.7	D4448	60/3	94=47×2	0.17	2.4	220	0.11	1	220	0.11	0.2
87	60	12	4	0.33	1.5	4.7	D4448	60/6	DMT2-79	0.07	4.8	470	0.065	1.7	470	0.065	0.25
88	60	12	6	0.22	2	4.7	D4448	60/6	DMT2-47	0.04	7.2	680	0.047	2.4	680	0.047	0.4

force Q₁ to saturate, causing the IC to deliver base current in excess of 0.7A to Q₁. This action triggers the IC's pulse-by-pulse current limit and protects the IC, Q₁, and the load from further excessive current. An output short circuit causes the IC to reduce its clock frequency, protecting D₁ and L₁ from high continuous peak current. The power dissipated in R₁, which can be a significant part of the total loss, subtracts from the dissipation in Q₁, allowing for a smaller heat-sink requirement. This dissipation is:

$$R_1(I_{OUT})(I_{OUT})(V_{OUT}/V_{IN}).$$

2. Choose R₂ to be small enough to quickly turn off Q₁ but not so small that it diverts much needed drive current away from Q₁ and causes early current limit. A value of 4.7Ω (the value that Table 1 uses) is a good trade-off value for most applications.

3. Choose Q₁ to be a fast switch with V_{CE} rating greater than 60V and I_{CE} rating of two times the desired current peak. This ratio generally provides a high beta over the working-current range. The D44H8 works well to more than 6A output in a TO-220 package and more than 2A in an SOT-223 package.

4. Choose D₁ to be a Schottky diode rated for the maximum values of V_{IN} and I_{OUT}. D₁ dissipates much of the total power loss when V_{IN} >> V_{OUT}, so look for a diode rated at less than 0.5V forward drop.

5. Choose L₁=47 μH/√I_{OUT} for V_{OUT}=3.3V, 68 μH/√I_{OUT} for V_{OUT}=5V and 150 μH/√I_{OUT} for V_{OUT}=12V. Choose the nearest L₁ value with a saturation and working current rating greater than I_{OUT}. Coilcraft's (www.coilcraft.com) SMT DO5022 family works well for output current to 1 or 2A, but you need larger cores for currents greater than 3A. You can tie these SMT inductors in series or in parallel to extend their use to 3 to 4A. They're also available in stacked-core versions for higher current use. Through-hole inductors, such as Coilcraft's DMT2-xx family, are physically larger but provide lower losses, especially for output current greater than 5A.

6. Choose C₁ for ripple-current rating and C₂ for low ESR. A minimum capacitance value for C₁=C₂/10≥100 μF×I_{OUT} works well at low current, but, as current rises to several amps, you need larger values to meet ESR and ripple-current re-

quirements. Ripple-current rating depends on several variables, but a conservative choice is half the maximum output current for C₁ and one-fourth the maximum output current for C₂. High ripple-current capability may require paralleling several capacitors for C₁. Select C₂ to have ESR less than 0.1Ω / I_{OUT} to keep the V_{OUT} peak-to-peak ripple less than 50 mV. Choose capacitors by looking at those targeting high-temperature use in switching power supplies with published ESR and ripple current ratings. Then, select a voltage rating higher by at least 50% than the expected operating voltage.

7. R₀, C_{SS}, and C_D are optional. You can leave these pins open if you don't intend to use them. You can shut off the circuit by pulling Pin 5 low and then turn it on again with soft-start by allowing Pin 5 to float high. Refer to the 2597 data-sheet graphs for C_{SS} and C_D values necessary to set the desired soft-start and power-good flag delay times.

Is this the best Design Idea in this issue? Select at www.edn.com.

IC maintains uniform bias for GaAs MESFETs

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

THE GATE-TURN-ON THRESHOLD voltage for GaAs MESFETs (gallium-arsenide metal-semiconductor field-effect transistors) varies considerably from part to part, even within a given lot. That behavior makes biasing difficult, especially if you want to design the device into a high-volume product. To overcome this

drawback, you can introduce a current sensor that monitors the bias current and provides feedback to the gate input (Figure 1). IC₁ combines a current sensor and an error amplifier. Intended as a power-control IC for power amplifiers, it senses the drain-source current, I_{DS}, at the source; compares and integrates the dif-

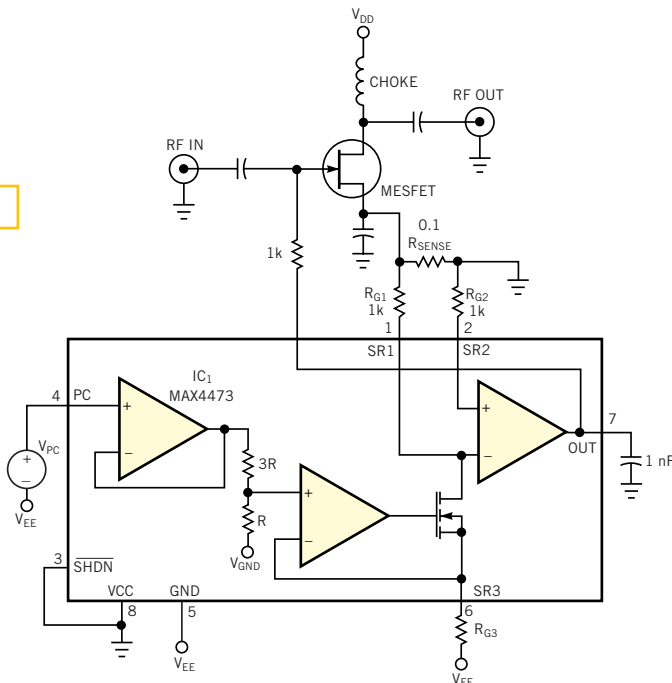
ference between voltage drops across R_{SENSE} and R_{G1}; and feeds back an output voltage to the MESFET gate. The feedback adjusts I_{DS} until the two voltage drops are equal, thereby achieving uniform source current, regardless of the MESFET's gate-threshold characteristics. The expression for drain-source current is:

$$I_{DS} = \frac{V_{PC} \cdot R_{G1}}{4 \cdot R_{G3} \cdot R_{SENSE}}$$

Current through R_{G1} depends on a voltage, V_{PC} , with respect to the negative supply, V_{EE} , applied to the power-control input at Pin 4. You can implement V_{PC} with a voltage divider, a reference, or a variable-voltage source. Because the gate voltage is negative with respect to the source, you must modify IC_1 's supply voltage to ensure a negative gate drive for the MESFET: Connect the V_{CC} pin to ground and the ground pin to V_{EE} . You can easily modify this uniform-bias circuit for biasing bipolar transistors and MOSFETs, as well.

Is this the best Design Idea in this issue? Select at www.edn.com.

Figure 1



A smart-bias IC ensures uniform bias for GaAs FETS in high-volume products.

Add gain to an absolute-value amplifier

Chuck Wojlaw, Catalyst Semiconductor, Sunnyvale, CA

THE ABSOLUTE-VALUE AMPLIFIER is a basic building block in test-and-measurement and signal-processing applications. The addition of a DPP (digitally programmable potentiometer) adds another dimension, G (gain), to this key circuit. Because the gain is programmable, you can use the circuit as an absolute-value amplifier ($G > 1$) or an absolute-value attenuator ($G < 1$). The single-supply

circuit in **Figure 1** comprises IC_1 , which is an inverting amplifier for positive-polarity signals only, and IC_2 , the summing amplifier. For the summing amplifier, R_1 represents a programmable, variable resistance. This resistance is modeled as $pR_2 = p(10\text{ k}\Omega)$, where p varies from 0 to 1/99 to 99/99 and represents the relative wiper setting from one end of the potentiometer (0) to the other end (1). For in-

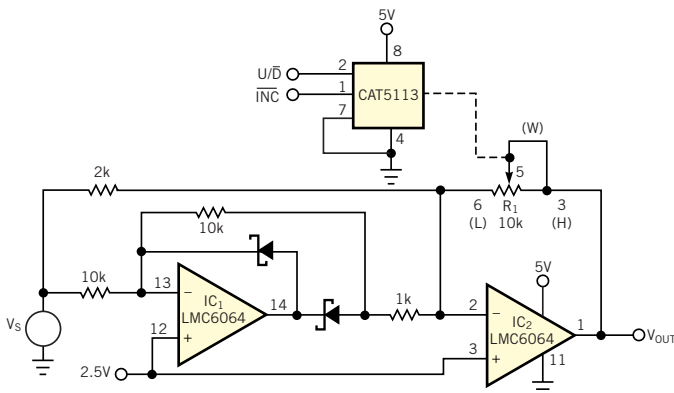
put voltages above the reference, for example, $V_s > 2.5\text{V}$ and for voltages below the reference, $V_s < 2.5\text{V}$, $V_{OUT} = 2.5\text{V} + |p5V_s| = 2.5\text{V} + |GV_s|$.

The potentiometer, a Catalyst 5113, has 100 taps and an increment/decrement interface. For this DPP, the circuit gain varies from 5/99 to 5. The measured accuracy of the circuit is approximately 1% for moderate values of gain (0.5 to 4) and for a characterized end-to-end resistance, R_{POT} . During power-up, the wiper goes to its stored value in non-volatile memory. This stored value establishes the default value of the gain after power-up. The basic idea for this absolute-value circuit came from **Reference 1**.

REFERENCE

1. Cipri, Teno, "Absolute-value comparator touts accuracy, size," *EDN*, March 7, 2002, pg 124.

Figure 1



Attenuate or amplify with this variable-gain absolute-value circuit.

Is this the best Design Idea in this issue? Select at www.edn.com.

Use a PIC for automatic baud-rate detection

Ross Fosler, Microchip Technology, Chandler, AZ

AUTOMATIC BAUD-RATE DETECTION IS desirable in many applications. Microchip's (www.microchip.com) standard USART module that the company embeds in most of its PIC microcontrollers lends itself to a simple and easily implemented automatic baud-detection scheme. The PIC-18FXX2 data sheet defines the following baud rate in bits per second:

$$X = \frac{F_{OSC}}{16 \times B} - 1; B = \frac{F_{OSC}}{16(X+1)}, \quad (1)$$

where X is the value for the baud-rate generator and F_{OSC} is the input clock frequency.

Figure 1 represents a general-case signal typically seen on the RX pin of a PIC microcontroller. The time, p, is the number of instruction cycles from the end of the start bit to the beginning of the stop bit. This definition allows you to relate baud rate, B, to the total time it takes for the RX pin on the microcontroller to see eight bits of data. Eight is a convenient figure for a binary machine. Basically,

$$p = \frac{8 F_{OSC}}{B \cdot 4}; B = \frac{2F_{OSC}}{p} \quad (2)$$

The term ($F_{OSC}/4$) is the instruction rate of a PIC microcontroller. The term $8/B$ is the eight bit-times that the RX pin sees. Relating the two baud-rate equations,

$$B = \frac{2F_{OSC}}{p} = \frac{F_{OSC}}{16(X+1)}; X = \frac{p}{32} - 1. \quad (3)$$

The simplified result leads to a simple equation that you can easily implement on a PIC microcontroller. Count the total numbers of instruction cycles for eight bit-times. Divide the result by 32. (In other words, shift the count right five times.) Add a rounding bit. Then, decrement the value by one. Finally, load the SPBRG register with the result to synchronize the PIC microcontroller to the incoming baud rate. It is important to select the right control signal so that the microcontroller samples the correct number of bits. For this implementation, the signal

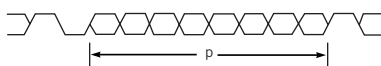


Figure 1 This bit stream is a general-case signal typically appearing on the RX pin of a PIC microcontroller.

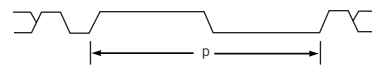


Figure 2 For the baud-rate-detection scheme, this waveform represents an ideal control signal.

in **Figure 2** is an ideal control signal. You take measurements from the rising edge, and the pulse is symmetric. **Figure 3** shows the simplified program flow for the baud-rate detection.

It is useful to know the valid frequency range for a baud rate, SPBRG value, and tolerable error. The following equation defines error as follows:

$$E(B_C) = \frac{B_C - B}{B}, \quad (4)$$

where B is the desired baud rate and B_C is the calculated or actual baud rate. Substituting **Equation 1** for B_C and using algebra leads to the following result:

$$F_{OSC} = (E + 1)(X + 1)(16)(B). \quad (5)$$

E is the error used to determine the maximum and minimum frequencies for a chosen baud rate and SPBRG value. For example, a good value for E would be 62%. Evaluating **Equation 5** for the high and low limits of error E yields a valid oscillator operating range. For most SPBRG values, common baud rates, and the most common clock frequencies, operating ranges overlap each other from one SPBRG to the next. Thus, the automatic baud-detection scheme synchronizes with the source for most of the common conditions. However, some errors and clock frequencies never have a valid SPBRG (X) value.

To approach this problem, you must compare the maximum frequency

for an SPBRG value with the minimum frequency of the next SPBRG. The value at which they're equal is the border between continuous and discontinuous operation for any given input frequency. The following two equations express this equality and the continuity barrier:

$$(E_H + 1)(X)(B)(16) = \quad (6)$$

$$(E_L + 1)(X + 1)(16)(B).$$

$$X_{LOW} = \frac{(E_L + 1)}{(E_H + 1) - (E_L + 1)}. \quad (7)$$

Thus, for any given frequency and a defined error, the automatic baud-detection scheme always generates a good SPBRG value if it is above X_{LOW} . Of course, you must select the frequency and baud rate such that SPBRG is less than or equal to 255, the largest value that SPBRG supports. For example, for a 2% error, the lowest SPBRG value before certain clock frequencies become a problem is 25. A bootloader is an excellent example of an application for this baud-rate-detection scheme. The simple implementation uses minimal resources. It synchronizes to a baud rate within one transmitted byte, and you can most likely successfully synchronize it to any standard baud rate, especially 9600 bps.

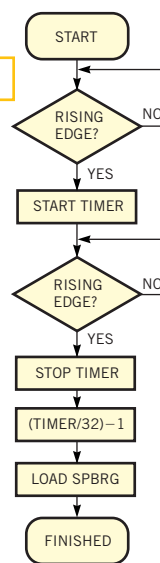


Figure 3 This program-flow diagram illustrates the principles of the baud-rate-detection technique.

Is this the best Design Idea in this issue? Select at www.edn.com.

Design low-duty-cycle timer circuits

Phil Rogers, Texas Instruments Inc, Rockwall, TX

DESIGNING ASTABLE CIRCUITS using the industry-standard 555 timer is a straightforward process when duty cycles are 50% or greater. However, you must overcome the many pitfalls of low-duty-cycle circuits to arrive at a desired result. Using only ideal components eases the design, but the components themselves are hard to obtain. Nonideal components get in the way of the easy-to-use standard equations and greatly multiply the tolerances. This Design Idea uses the TLC555 CMOS timer. You can use other versions of the popular 555 timer with appropriate variations in the given parameters. For a standard, greater-than-50%-duty-cycle, low-frequency design (Figure 1), you would use the following design equations:

$$t_H = C \cdot (R_A + R_B) \cdot \ln(2);$$

$$t_L = C \cdot R_B \cdot \ln(2);$$

$$\text{DUTY CYCLE} = \frac{(R_A + R_B)}{(R_A + 2R_B)}$$

Charging current for the timing capacitor flows through R_A and R_B until the capacitor voltage reaches the upper threshold voltage of $0.667V_{CC}$. The capacitor then discharges through R_B and an internal transistor to the lower threshold voltage of $0.333V_{CC}$. Because R_B is present in both the charging and the discharging cycles, you can't implement duty cycles lower than 50% in this configuration. These idealized equations also ignore several factors that slightly degrade the results for the higher range of duty cycles but greatly influence the results of low-duty-cycle designs. These factors include propagation delays and the on-resistance of the internal discharge transistor. All these factors are supply-voltage-dependent. Another factor for low-duty-cycle designs that does not apply to high-duty-cycle designs is the effect of the R_B bypass diode, D_1 (Figure 2), required to implement the design.

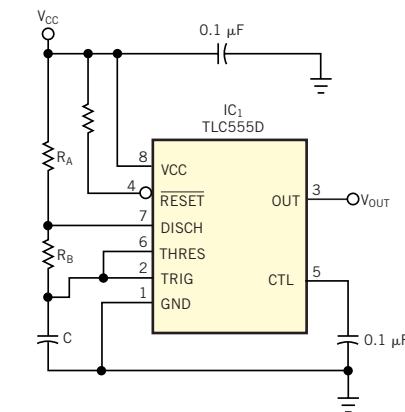


Figure 1 This classic 555-based timer is valid only for duty cycles greater than 50%.

Adding a bypass diode across R_B allows for designs with duty cycles lower than 50%. During the charging cycle, current flows through R_A and bypasses R_B through the diode. During discharge, current flows through R_B and the internal discharge transistor as usual. Because R_B is now present only in the discharge cycle, you can tailor the duty cycle to any desired point over the full range. Again, using ideal components, the timing equations are simple:

$$t_H = C \cdot R_A \cdot \ln(2);$$

$$t_L = C \cdot R_B \cdot \ln(2);$$

$$\text{DUTY CYCLE} = \frac{(R_A)}{(R_B)}$$

The factors you must consider in obtaining a design that agrees with calculations include the:

- diode forward voltage,
- propagation delays,
- discharge-transistor on-resistance,
- ratio of R_A to on-resistance, and
- leakage resistance of the control-pin capacitor.

Diode forward voltage depends on the

current flowing through the diode. This current can range from a few hundred microamps to tens of milliamps. For a fixed design, you can obtain this voltage from manufacturers' curves or actual measurements you make by applying the desired current through the diode. You can also use the diode equation:

$$I = I_S(e^{qV/kT} - 1).$$

Or, in terms of voltage:

$$V_F = \frac{1}{0.026} \cdot \ln\left(1 + \frac{I}{I_S}\right) = 38.46 \cdot \ln\left(1 + \frac{I}{I_S}\right).$$

This voltage subtracts from the charging voltage during the charging cycle and affects the charge-ramp time. Propagation-delay times from the THRES (threshold) and TRIG (trigger) inputs to DISCH (discharge) add directly to the period. These delays depend upon supply voltage. The formulas for the propagation delays (in nanoseconds) are:

$$T_{PHL} = -0.0162V_{CC}^5 + 0.8207V_{CC}^4 - 16.205V_{CC}^3 + 155.62V_{CC}^2 - 31.88V_{CC} + 1558; T_{PLH} = -0.0102V_{CC}^5 + 0.5044V_{CC}^4 - 9.6825V_{CC}^3 + 89.622V_{CC}^2 - 401.04V_{CC} + 807.97.$$

Discharge-transistor on-resistance also varies with supply voltage. This resistance affects the discharge current. Also, when you use low-value resistors for R_A (for low-duty-cycle designs), the combination of R_A and the on-resistance yields a voltage divider that affects the discharge voltage. The on-resistance formula for resistance in ohms is:

$$R_{ON} = 59.135V_{CC}^{-0.8101}.$$

Typically, you'd place a small capacitor on the control pin that connects to the upper internal-divider node. This capacitor has only a slight effect on the threshold-trigger voltages. The leakage resistance of the ceramic capacitor is approx-

imately 9 MΩ. This value is high but still accounts for approximately a 1.5% drop in the trigger voltages because of the 80-kΩ divider resistors that the window-

comparator circuit uses. When you take all the cited parameters into account, the design equations become considerably more complicated:

These equations include all the known parameters to obtain a nominal design using the TLC555 timer. Tolerances in each of the parameters cause additional variations that you must consider. In addition, you must consider the effects of temperature variations. After you obtain all this knowledge, the simple 555 timer presents a major math problem. However, thanks to modern computers, you can eliminate much of this tedious math using an Excel spreadsheet. It shows the results of calculations both with and without the bypass diode and includes the tolerancing parameters. You can download the spreadsheet from the Web version of this Design Idea at www.edn.com.

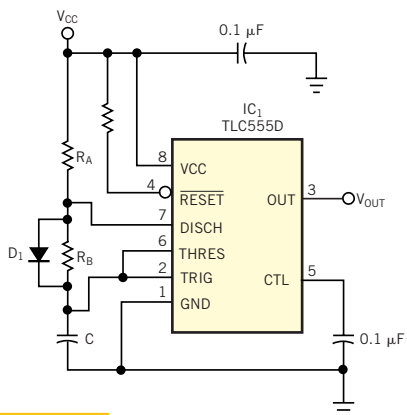


Figure 2

The simple addition of a bypass diode makes this timer circuit valid for low duty cycles.

$$t_H = C \cdot R_A \cdot$$

$$\ln \left[\left(3 - e^{-t_{PHL}/(R_{ON} \cdot C)} \right) \cdot \left(\frac{2 \cdot V_{CC}}{(2 \cdot V_{CC} - 3 \cdot V_F)} \right) \right] +$$

$$t_{PHL};$$

$$t_L = C \cdot (R_B + R_{ON}) \cdot$$

$$\ln(3 - e^{-t_{PHL}/(C \cdot R_A)}) \cdot 2.38 \cdot$$

$$\left(1 - \frac{\left[1 - \left(\frac{3 \cdot R_{ON}}{(R_A + R_{ON})} \right) \right]}{2 - \left(\frac{3 \cdot R_{ON}}{(R_A + R_{ON})} \right)} \right) + t_{PLH}.$$

Is this the best Design Idea in this issue? Select at www.edn.com.