



Pleased to
meetcha—NOT

“Sort of the spam
world meets the
virus world.”

—software developer
and computer-security
expert Richard Smith
on the dramatic spread
of the SoBig worm,
in *The Boston Globe*,
Aug 27, 2003

Bluetooth gets DSP backup

By Nicholas Cravotta

CAMBRIDGE SILICON RADIO has launched its BlueCore3 Bluetooth family, supporting Version 1.2 of the Bluetooth specification, including all optional features of the standard. The BlueCore3-Multimedia has an integrated programmable DSP

supporting enhanced audio and echo cancellation for applications such as wireless stereo headphones. The device includes a 16-bit stereo codec with a dual ADC/DAC for stereo output and integrated amplifiers for driving a microphone and speakers.

The BlueCore3-ROM targets low-cost, high-volume applications, such as Bluetooth-enabled cell phones. New built-in self-test routines speed production testing. The

BlueCore family also supports the ability to adapt the page-scan interval of Bluetooth to that of mobile phones, thus increasing the battery life of such devices.

Currently available, the BlueCore3-Multimedia comes in a 10×10-mm, 96-ball LFBGA package and sells for \$8 (one) in sample quantities. The BlueCore3-ROM is available in chip-scale, 4×4-mm; BGA; and RF Plug and Go packaging, which integrates



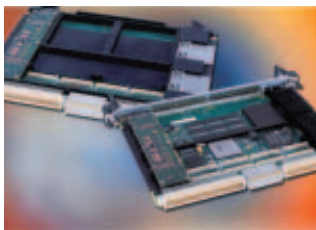
The BlueCore3 family of Bluetooth devices is version 1.2 qualified and comes either with an integrated DSP for advanced applications or in a ROM version for low-cost, high-volume applications.

matching circuitry so that you can directly connect an antenna to the device. It costs less than \$5 (production volumes).

►Cambridge Silicon Radio, 1-972-238-2300, www.csr.com.

Rugged single-board computer includes two 1553B interfaces

TARGETING AVIONICS and harsh environment applications, the SVME/DMV-182 single board computer from Dy 4 Systems includes an integrated dual-channel MIL-STD-1553B interface in a single-slot VMEbus card. A unique IPM (interface-personality module) allows you to integrate one or two 1553 channels onto the SVME/DMV-182 without impacting the two PMC-mezzanine-module sites. With features independently selectable for each channel, the module supports bus-controller, remote-terminal, and bus-monitor modes. The IPM also supports the full range of 1553 variants, including 1553A, 1553B Notice 2, and Standard NATO Agreement 3838 protocols. Dy 4's 1553 driver software and application-program interface are compatible



The new SVME/DMV-182 single-board computer includes a dual-channel MIL-STD-1553B interface in a single-slot, rugged VMEbus form factor.

with the VxWorks and Integrity real-time operating systems.

The base SVME/DMV-182 single-board computer features dual PowerPC 7455/7457 processors that operate as fast as 1.3 GHz, as much as 1 Gbyte of DDR SDRAM with ECC, a 128-Mbyte flash memory, six serial ports, two USB 2.0 ports, and two 64-bit PMC sites on independent PCI buses; one bus supports 66-MHz PCI-X, and the other offers 133-MHz PCI-X. The SVME/DMV-182 is available now. The SVME/DMV-182 with 1553 will be available in the fourth quarter. Prices for the SVME/DMV-182 start at \$11,950.

—by Warren Webb

►Dy 4 Systems Inc, 1-613-599-9199, www.dy4.com.

PXI modular instruments target mixed-signal test

NATIONAL Instruments' new mixed-signal test suite, an ensemble of PXI modular instruments, aims at a target that has long tantalized developers of instrumentation for verifying IC designs and for testing the devices in production. Almost all who examines the related problems of design verification and production test begins by asking why test programs that design engineers develop for verification shouldn't also be usable in production. The answer is simple: Verification programs gather quantitative information on device performance—often under “corner-case” conditions—for example, at simultaneous extremes of supply voltage and operating temperature. Production-test programs implement go/no-go tests to establish whether devices are good enough to ship. Verification programs collect voluminous data; device throughput is, at best, a secondary consideration. Although production tests can't tolerate inaccurate results, throughput is the prime consideration.

NI believes that its new products can end development

of separate verification and production-test programs because the modules' new SMC (synchronization-and-memory-core) architecture combines with PXI systems' enormous computing power to enable verification programs to run much faster than do go/no-go tests that use conventional instrumentation. Moreover, an interactive digital-waveform editor enables quick creation of test patterns as well as importation of patterns from simulation tools and older test programs. As impressive as these claims are and notwithstanding NI's insistence that its customers demand the capability, the company and its customers must still demonstrate that test programs created for



The mixed-signal test suite includes seven waveform-digitization, -generation, and -support modules in single-width PXI format.

design validation can meet production-test needs.

The product line includes the 20-channel NI PXI-6551 and -6552 50- and 100-MHz digital-waveform generators/analyzers, which start at \$4995 and \$6995, respectively. A more familiar name for such instruments is “digital-pattern generator.” All channels are bidirectional, so the units can both source and monitor parallel signals and compare received signals with expected data. You can order the units with as much as 64 Mbits of memory behind each pin. Looping and branching capabilities extend the memory depth virtually without limit.

Other units include the two-channel, 100M-sample/sec, 14-bit PXI-5122 digitizer, which starts at \$4995; the 16-bit 5421 arbitrary-waveform generator, starting at \$4995; the 5404 clock and frequency generator beginning at \$1495; and the 500-MHz 2593 switching module beginning at \$1595. A timing and synchronization module will be available in the fourth quarter of 2003.—by Dan Strassberg
▶National Instruments, 1-800-258-7022, www.ni.com.

SYNTHESIZABLE 6811 MICROCONTROLLER SUPPORTS MULTIPLE TOOLS

Synopsys has added a synthesizable and configurable model of the 6811 8-bit microcontroller to its Designware library. The 6811 is an industry-standard microcontroller with broad software-tool-chain support. Designers migrating from a discrete implementation to a system-on-chip design can use the macrocell to speed the new implementation.

The development of the 6811 macrocell followed the guidelines in the *Reuse Methodology* manual, and the development team also tested the part as a component of the DesignWare BlueIQCore, which implements the full Bluetooth-baseband controller and link manager. The DesignWare library includes the 6811 MacroCell. Customers with a current license can access the new macrocell for free. For more information on the DesignWare library visit www.designware.com.

—by Gabe Moretti

▶Synopsys, 1-650-584-5000, www.synopsys.com.

DILBERT By Scott Adams



▶ Sales of cell-phone handsets worldwide rose 12% in the second quarter of 2003, according to Gartner.

NSE ups TCAM ante to 266 million searches/sec

THE AYAMA 10000 NSE (network-search-engine) family from Cypress Semiconductor increases TCAM (ternary-content-addressable-memory) search rates for multiprotocol-packet

classification and forwarding to 266 million searches/sec for applications requiring wire-speed packet-search capabilities at 10 Gbps or greater.

Leading the Ayama 10000 NSE family is the CYNSE10512, a 512k-entry, 18-Mbit device. Other members include the 256k-entry, 9-Mbit CYNSE10256 and 128k-entry, 4.5-Mbit CYNSE10128 devices. Mini-Key power-management capability reduces power consumption by en-

gaging only those portions of the NSE array that contain entries of interest. The Soft Priority table-management feature helps maintain data integrity at wire speeds by dynamically prioritizing entries for LPM (longest prefix matching) in Layer 3 applications, thus eliminating the latency associated with routing-table updates. Additional features include per-bit masking and parity at the core and I/O to ensure data integrity throughout the device.

Cypress' new software platform, Cynapse, provides a unified software environment for application simulation and development across all Cypress network search engines. Diagnostic tools aid in the development of reliable code. The platform also provides reference applications, simulation models, APIs, and drivers.

All Ayama 10000 devices are currently available for sampling. The CYNSE10512

costs \$275 (10,000), and volume production is slated for the first quarter of 2004. The CYNSE10256 costs \$135 (10,000), the CYNSE 10128 costs \$75 (10,000), and volume production is slated for both these devices in the sec-

ond quarter of 2004. The Cynapse software-development platform is free to silicon customers.

—by Nicholas Cravotta

► **Cypress Semiconductor**, 1-408-943-2600, www.cypress.com.

TOOL ADDRESSES ANALOG-, MIXED-SIGNAL DESIGNS

Mentor Graphics has added the ICAssemble tool to its IC Station product. The tool allows designers to perform top-down floorplanning, advanced interactive and automatic routing, and chip assembly. Engineers can now plan, implement, and connect blocks within a physical-layout environment. Digital-logic designers can now avail themselves of silicon virtual prototyping to obtain quick feedback of the physical characteristics of their designs—a luxury that analog engineers previously lacked. Such engineers can use ICAssemble to visualize the physical structure of the analog blocks, thus increasing productivity.

The tool's floorplanner supports chip planning based on global connectivity and design constraints. Starting with a hierarchical description of the connectivity, designers can partition the chip, estimate block sizes, and then place the blocks and assign pin locations to minimize congestion and wire lengths for critical signals.

The IRoute interactive router helps designers in the planning stage by routing power buses and critical signals to meet timing constraints. IRoute adheres to constraints on shielding, spacing, widths, and directions of wires and respects the design hierarchy. Another part of the product, the ARoute interactive rip-up and reroute tool allows bulk routing of nets, which it selects by region or group. It obeys design-rule-checking rules, and, using appropriate constraints on wire spacing, widths, and shielding, it can produce results that meet signal-integrity requirements. The product sells for \$75,000. It is available on Linux, Sun Solaris, and HP-UX platforms.

—by Gabe Moretti

► **Mentor Graphics**, 1-503-685-8000, www.mentor.com.



The Ayama 10000 NSE family of TCAM-based search engines provides as many as 266 million searches/sec.

Shorten FPGA-integration time in pc-board design

DESIGNERS TYPICALLY use schematic diagrams to design pc boards and require a symbol for every component on the board. Today's large pc boards present a challenge because they may have more than 1000 pins, making it practically impossible to use a traditional symbol. To address the problem, Mentor Graphics has introduced FPGA BoardLink to automate the integration of the FPGA on the board.

The tool allows you to schematically represent large devices by partitioning them into smaller symbols. The tool accomplishes symbol fracturing through a table-driven method. It then automatically merges and maps the partitions to the FPGA package for pc-board layout and simulation. When you change the FPGA that results in a pinout change, the tool automatically updates the pinout assignments for each symbol or

partition based on the FPGA place-and-route results.

FPGA BoardLink is available free to Mentor's pc-board-design-solution customers. Mentor integrates the tool with Board Station, Expedition, and FPGA Advantage, and it also supports Xilinx's ISE Alliance, Altera's Quartus, and Actel's MaxPlus II tool.—by Gabe Moretti
► **Mentor Graphics**, 1-503-685-8000, www.mentor.com.

Tool targets yield optimization

PROCESS VARIATIONS at nanometer levels significantly impact yields. Because simulation and nominal optimization tools analyze a design for a

fixed set of parameters, they fall short of predicting true parametric yield based on process variations. ChipMD has introduced the DesignMD tool, which includes deterministic-yield-optimization technology to aid engineers in analyzing and understanding the factors that contribute to yield. Designers using the tool can optimize the design to achieve a higher yield across all ex-

tremes of the process parameters and for all operating conditions.

DesignMD uses standard Spice netlists as input and outputs the equivalent netlist with optimized design device sizing. Users can select from several analysis options. These include yield optimization to automatically size transistors and other passive devices to achieve higher

yields and sensitivity analysis to discover in which direction each design parameter, such as width and length of a transistor or capacitance or inductance value, influences a performance parameter. The product also offers an extended Monte Carlo analysis to evaluate yield and performance variations with respect to variations in process and operating parameters by determining the worst-case operating parameters at each process point

The product also determines the worst-case point and the distance of that point

from nominal, using a deterministic algorithm to identify the achievable performance parameter for the target yield. Designers can also identify devices within a circuit that cause mismatch problems and quantify the impact of the problem on the yield. The tool automatically optimizes a design to meet the required yield specification by changing design parameters. A minimum configuration of ChipMD starts at \$50,000 for a time-based license.—by Gabe Moretti

► **ChipMD**, 1-408-725-9580, www.chipmd.com.

Tiny Wi-Fi chip debuts

NOW THAT 802.11 or Wi-Fi wireless LANs have pervaded the notebook PC, the attention of the IC vendors turns to other potential Wi-Fi hosts. Many PDA users add Wi-Fi capability via CompactFlash 802.11 cards, and such connectivity is valuable at conventions. Consumers may also demand Wi-Fi in cell phones, MP3 players, digital cameras, and other tethered appliances. In the case of digital cameras, for instance, Wi-Fi would allow transfer of photos from a camera to a PC on the wireless network at much higher speeds than Bluetooth would allow.

However, to effectively address small portable devices, such as PDAs and cell phones, system designers need physically more compact Wi-Fi implementations than those that notebook PCs use. Early notebook users added Wi-Fi via PC Cards. Now, many notebooks embed the Wi-Fi capability. Generally, system designers buy Wi-Fi modules in the mini PCI form factor rather than mounting the capability on the main-system pc board. The module approach allows system designers to avoid the complex analog

design of the RF products. Moreover, regulatory agencies can certify the modules separately from the notebook PC, removing that hurdle for PC vendors.

Mini PCI modules measuring 50×60 mm, however, are still too large for PDAs and other small devices. Wi-Fi implementations require much of the Mini PCI real estate, so vendors can't just use a smaller module, and discrete analog components occupy much of the module's area.

Broadcom claims to be the first company in line with a smaller module design for 11-Mbps 802.11b networks. The company's new AirForce OneChip addresses the size issue in two ways. First, the chip integrates both the digital baseband and the analog radio. Broadcom had previously shipped the radio chip using a CMOS digital process employing the company's Direct Conversion RF technology. Now, Broadcom includes the Direct Conversion function, the baseband, and many of the discrete components in the IC. A Wi-Fi module that uses the new chip requires only 30 discrete parts, whereas the company's two-chip

module required 200 such parts. This approach decreases the bill of materials for the discrete components by \$5.

Assuming that Broadcom can deliver the OneChip, and it claims to be shipping module reference designs to close partners, the new IC will enable 14.8×26.5-mm modules. The design is small enough to go into SD Cards, PDAs, and cell phones. Moreover, the new design delivers better sensitivity for improved performance, along with huge power savings: Standby power decreases from 600 to 6 mW. The device costs approximately \$10 cost in high volumes and will cost less in implementations lower than Mini PCs. A few notebook-PC vendors may integrate the new module, although the PC industry is largely moving to faster 802.11g and 802.11a technologies. Broadcom claims that it will later implement a single-chip 802.11g variation. Meanwhile, it has also packaged both 802.11g and Bluetooth in the same 14.8×26-mm footprint and will sell that module for around \$14 in volume.—by Maury Wright

► **Broadcom Corp**, 1-949-450-8700, www.broadcom.com.

► The worldwide smart-antenna market will reach \$1.6 billion in sales by 2008, according to a study from Visant Strategies.

Revolutionary new transmission scheme overcomes unreliable networks

DIGITAL FOUNTAIN has announced the availability of its Meta-Content technology for improving the reliability of data transmission over unreliable links and through congested networks. Wireless networks, for example, can experience loss of consecutive blocks of data due to interference from other nearby wireless networks. Another example, TCP, ramps down the data rate when it detects congestion to reduce the number of dropped packets. However, TCP determines congestion by measuring how long acknowledgments take to arrive; thus, packets traveling long distances trigger a reduced data rate, even though there may be little actual congestion.

Using traditional transmission schemes, lost or dropped packets add a significant amount of latency to transactions through acknowledgment time-outs and packet resends. Using Meta-Content packets, a transmitting node sends data until the receiving node has received enough Meta-Content packets to reconstruct the original data. It doesn't matter which packets a node receives, as long as the node receives enough packets. Thus, the receiving node needs to send an acknowledgment only after the entire transmission has completed.

Meta-Content technology accomplishes this task by encoding packets, effectively XORing them together in varying degrees. For example, consider a 100-packet-long message. A first-degree Meta-Content packet contains one of these packets in its original form. A second-degree Meta-

Content packet contains any two of the packets XORed together, and so on.

A first-degree, or source, packet immediately yields the original packet it encodes. The decoder then uses this packet to unlock other Meta-Content packets or to reduce them to a lower degree. For example, consider a second-degree packet comprising original packets 5 and 47 XORed together. If either packet 5 or packet 47 arrives as a first-degree packet, the decoder can use it to recover the other packet. For a third-degree packet, you need any two of the packets to recover the third.

Through a random mix of degrees and original-packet combinations, a Meta-Content decoder collects packets as they arrive and begins to unlock them or reduce their degree as it recovers individual packets. The decoder keeps receiving Meta-Content packets until it has recovered the entire message. With 5% overhead, in this case 105 packets, there is a 10^{-13} chance you will recover all 100 original packets.

Each Meta-Content packet

adds a header describing which original packets it used to encode the packet. Because individual packet acknowledgments are unnecessary, Meta-Content can send packets using UDP to reduce handshaking overhead and latency.

Digital Fountain has implemented the Meta-Content decoder such that the memory to decode the message is the size of the original message; the decoder holds and recovers packets in the same memory it uses to hold the final received message. When a new Meta-Content packet arrives, the decoder checks the header to see whether it has recovered those original packets in the Meta-Content packet; if so, the decoder does not need to keep the packet.

Meta-Content technology also enables broadcast of data over unreliable links. In a traditional architecture, broadcast is difficult because some nodes may receive a packet, and others may not. With Meta-Content packets, even though each node may receive a different combination of packets, each node receives enough packets.

Meta-Content occupies 50 to 200 kbytes and is currently available for Solaris, Linux, Windows, VxWorks, and Brew on Intel x86, ARM, MIPS, and Hitachi (SH4) architectures. The API is in C; source code is not available. The technology is available in licensable objects, including DFCore, which handles encoding/decoding of meta-content; DFLive, which protects live streams of data by outputting protected code for the application to feed down the wire; and DF.Sockets, which is built on DFCore and includes encoding and transmission, such as transmitting UDP over TCP/IP. Transmission rates range from 2-Mbps T1 to 622-Mbps OC-12.

Available now, Meta-Content technology has a two-part license. The development license, including rights for development, testing, and demonstration, is \$25,000. The distribution license is a royalty per unit, based on volume or speed of data.

—by Nicholas Cravotta

► **Digital Fountain**, 1-510-284-1400, www.digitalfountain.com.

HDMI-compliance spec spurs interoperability

The HDMI (High-Definition Multimedia Interface) founders, comprising Hitachi, Matsushita Electric (Panasonic), Royal Philips Electronics, Silicon Image, Sony Corp, Thomson, and Toshiba, released the final 1.0 Compliance Test Specification for HDMI, an all-digital consumer-electronics interface combining high-definition video and multichannel audio with a bandwidth as high as 5 Gbps. The spec allows HDMI developers to test and verify device compliance and interoperability with other vendors' devices. Vendors must submit devices in source, sink, repeater, or cable categories. Authorized testing centers Silicon Image in Sunnyvale, CA, and Matsushita in Osaka, Japan, are currently accepting products for testing. Devices must pass compliance testing to bear the HDMI logo. Manufacturers themselves can test subsequent products. The spec is available for HDMI adopters to download at the organization's Web site.—by Nicholas Cravotta

► **High-Definition Multimedia Interface**, www.hdmi.org.

Software/hardware-tool kit reduces test-development time by 99%

IT'S EASY to become enamored of “charismatic” technologies—say, rewriteable DVDs that store 9.4 Gbytes—and overlook bread-and-butter inventions that can change your working life. Agilent's latest product, Test Automation Kit, might

have a boring name, but it can change the working lives of many engineers.

Agilent has demonstrated that its \$1995 kit, which includes both software and hardware, reduces to approximately an hour the time it takes to perform a group of necessary but tedious and unglamorous tasks that currently consume an average of 100 hours. The tasks

relate to setting up and configuring test instruments and ensuring that they accurately



Although the Test Automation Kit consists of some pedestrian-looking little boxes, cables, and a CD, it can completely transform and shorten by approximately 99% the heretofore-tedious task of configuring instruments and checking out test systems.

measure the correct quantities. The kit's value doesn't lie primarily in production test-

ing, says Agilent; the product's main use is in design labs in setups whose main purpose is characterizing and verifying the performance of products under development.

The kit automatically loads software drivers and configurations and verifies approximately two dozen of the manufacturer's most popular instruments. It supports voltmeters, function generators, counters, power supplies, signal-switching units, and oscilloscopes. The kit's components include a USB-to-IEEE 488 converter, the manufacturer's Test Express software, a test module and wiring harness, 200 program examples, and two hours of

telephone consultation that you can schedule with a systems expert. The kit also in-

cludes facilities for users to extend the list of supported instruments to other Agilent products and to products of Agilent's competitors.

Although many customers own working ensembles of instruments to which they can add the kit and immediately begin reaping its time savings, Agilent also offers two instrument ensembles that include the Test Automation Kit. The economy ensemble, which costs less than \$10,000, includes a multimeter, a relay multiplexer, a function/arbitrary-waveform generator, a frequency counter, a power supply, and cables. The high-capacity ensemble, which costs less than \$20,000, adds more signal-switching capability, an IEEE 488 interface module, an oscilloscope, and an equipment rack.

—by Dan Strassberg

► **Agilent Technologies**, 1-800-452-4844, www.agilent.com/find.kit.

Device integration targets telematics

MOTOROLA's MPC5200, an MPC603e PowerPC processor core, integrates Ethernet, CAN (controller-area-network), USB, IIC (inter-IC), IIS (inter-IC sound), SPI, J1850, ATA, PCI, and AC97-codec interfaces targeting telematics and industrial applications. The processor core includes a double-precision floating-point unit, a DDR-memory controller, a BestComm DMA controller, and 16 kbytes of instruction and data cache. It consumes 850 mW of power while operating at 400 MHz.

Development tools for the MPC5200 include the Total5200 development system and the Lite5200 evaluation board. The Total5200 development system includes an integrated LCD with a resistive touchscreen, a Bluetooth-ready

audio-subsystem daughtercard, 64 Mbytes of SDRAM, 64 Mbytes of flash memory, and the IBM Websphere Studio Device software-development kit. The Lite5200 evaluation board includes evaluation-version board-support packages for Green Hills Integrity, MontaVista Linux, and Wind River and VxWorks; a 45-day license for Metrowerks CodeWarrior; and two emulation probes. The 400-MHz MPC5200 is currently available for sampling, operates at -40 to +85°C in a 272-pin package, and will become available in late 2003 for \$22.50 (10,000). The company plans to later introduce a 264-MHz MPC5200 in a -40 to +105°C package.—by Robert Cravotta

► **Motorola**, www.motorola.com/semiconductors.

► According to Gartner, Nokia leads the cell-phone market with a 35.9% share Motorola follows with 14.6% of the market.