

Figure 3 The waveform at IC<sub>2</sub>'s differential-clock pins results when R<sub>1</sub> and R<sub>2</sub> are 0Ω and R<sub>3</sub> is unconnected. When the differential signals are driving two loads (as they are in this and the following three figures), the series resistors and the termination resistors could degrade the signals in rise time, fall time, and waveform shape if you use inappropriate values.

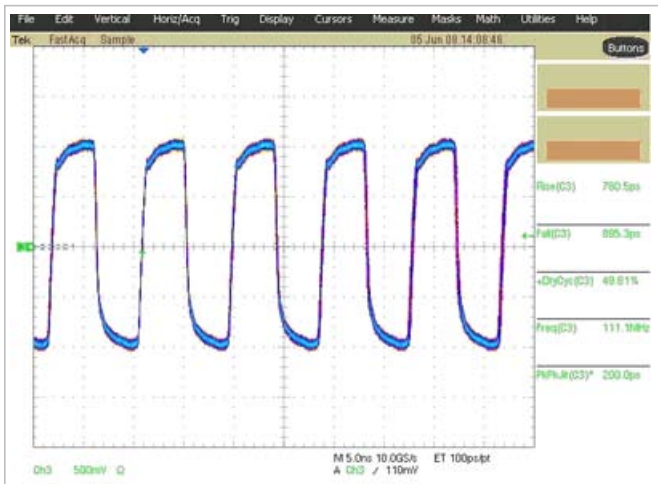


Figure 4 The waveform at IC<sub>3</sub>'s differential-clock pins results when R<sub>1</sub> and R<sub>2</sub> are 0Ω and R<sub>3</sub> is unconnected.

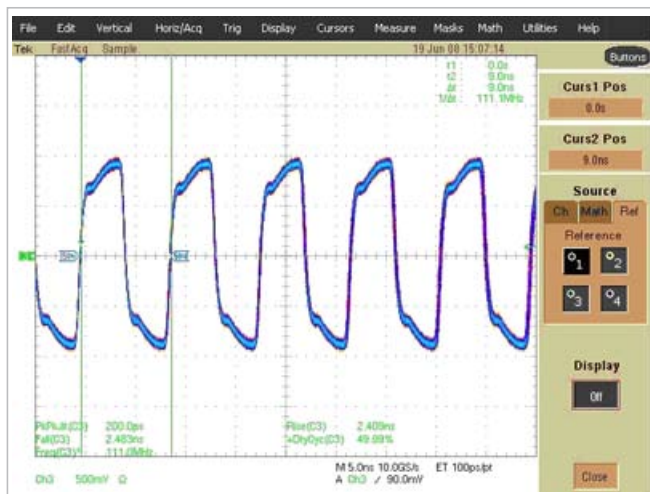


Figure 5 The waveform at IC<sub>2</sub>'s differential-clock pins results when R<sub>1</sub> and R<sub>2</sub> are 25Ω and R<sub>3</sub> is 120Ω.

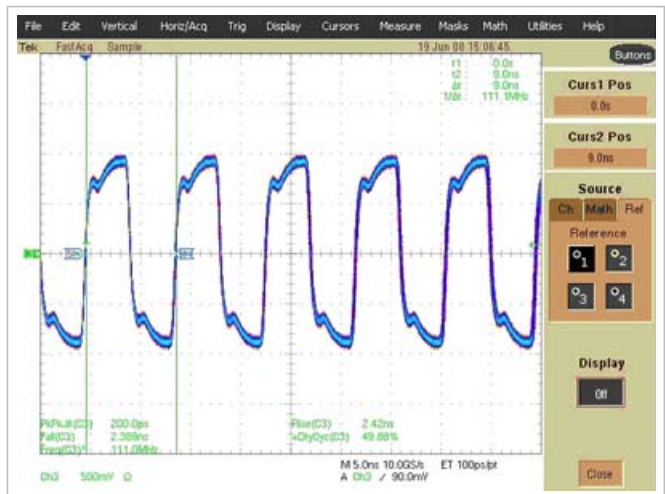


Figure 6 The waveform at IC<sub>3</sub>'s differential-clock pins results when R<sub>1</sub> and R<sub>2</sub> are 25Ω and R<sub>3</sub> is 120Ω.

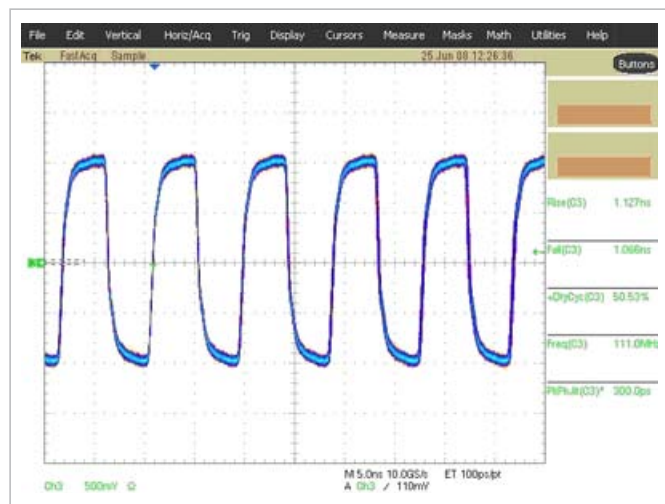


Figure 7 This waveform at the differential signal results when you use DDR chip IC<sub>2</sub> only. Comparing this waveform to those in figures 3 and 4 shows that the quality of the differential signals that drive two loads is as good as when they drive a single load. Hence, the differential-clock buffer is unnecessary in this case, greatly reducing system cost.