

Advanced Micro Devices

THE ÉLANSC520 MICROCONTROLLER COMBINES a 32-bit, low-voltage Am5x86 CPU with a complete set of integrated peripherals suitable for both real-time and PC/AT-compatible embedded applications. The device can run Windows NT embedded and features a 32-bit PCI bus; a 32-bit SDRAM interface; and AMDebug, a full-featured in-circuit-emulation capability.

Integrated peripherals: Interfaces exist for a DRAM controller, PC/AT peripherals, UART, synchronous serial ports, and communication-specific peripherals. The device includes a 16-kbyte write-back cache, a floating-point unit, and variable bus sizing.

Development tools: The development environment includes a JTAG port to support debugging. Most embedded RTOSs have been ported to and natively support the development platform.

Agilent Technologies

THE AGILENT AAEC-2000 is a high-performance, low-power, integrated system chip, based on the ARM920T microprocessor, designed to be the heart of a Personal Multimedia Digital Assistant. It includes a variety of external interfaces to support wireless Internet devices, MP3 players, and smart phones. The AAEC-2000's integrated architecture helps minimize chip count, footprint, and power consumption for these applications.

Power management: A programmable PLL and flexible clocking scheme fine-tune and match the processor's performance with external memory devices. The internal clock and state controller turns off the clocks to unused blocks, allowing the system to switch between run, suspend, and sleep modes. A separate video-bus subsystem eliminates bus contention for screen refreshes, reducing the need for off-chip frame buffer accesses.

Special instructions: The AAEC-2000 supports the standard ARM V5 and Thumb instruction set.

Integrated peripherals: The AAEC-2000 has interfaces are provided to connect to USB hosts, AC'97 codec, multimedia cards, audio output, synchronous serial devices, smart cards, three UARTs, an IrDA, and a keyboard. An external memory interface allows connection to static- and dynamic-memory devices, compact flash, PCMCIA, and synchronous memory. It also includes a smart-battery interface and LCD controller.

Development tools: The companion AAED-2000 Development System provides the tools for creating, testing, and evaluating systems based on the AAEC-2000 Information Appliance Processor. The development system's full set of I/O capabilities facilitates prototyping of all major elements of a mobile information appliance. You can use the self-contained and portable unit for mobile demonstrations and testing.

Alchemy Semiconductor

Alchemy Semiconductor's Au1000 and Au1500 are SoC based on the MIPS32 instruction set. Designed for maximum performance at very low power, they run at up to 500 MHz with power dissipation at less than 0.5 W (Au1000) to 0.7 W (Au1500) for the 400 MHz versions. In addition to a PCI 2.2 controller on the Au1500, both devices have integrated on-chip memory controllers and Internet access peripherals. They run a variety of operating systems, including Windows CE, Linux and VxWorks. The integration of peripherals with Alchemy Semiconductor's unique, high performance, MIPS-compatible core support lower system cost, smaller form factor, and lower system power requirements at multiple performance points.

Power management: Power-saving modes include idle, sleep, and pseudostatic design to 0 Hz.

Integrated peripherals: Peripheral support includes two 10/100 Ethernet controllers, USB device and host, up to four UART's, IrDA, AC'97 controller, I²S, two synchronous serial interfaces, as many as 48 general-purpose I/Os, as many as 22 dedicated I/Os, and a 33- or 66-MHz, 32-bit, PCI 2.2-compliant controller on the Au1500 device.

Development tools: A complete MIPS32-compatible tool set, numerous third-party compilers, assemblers, and debuggers support development efforts.

Altera

NIOS IS A PIPELINED RISC ARCHITECTURE, with a compiler-friendly instruction set that achieves 33- to 80-MHz operating speed and executes most instructions in one clock. The Nios soft—core, 16- or 32-bit-configurable processor supports all of Altera's look-up-table programmable logic devices. The ALU, register file, and memory interface are all either 16 or 32 bits, respectively. Both variants use 16-bit instructions. Users may add as many as five custom instructions to the ALU. Nios includes several soft-core peripherals that connect to the processor using a bus-fabric architecture that allows multiple bus masters to operate simultaneously. The architecture automatically generates arbiters for memory or peripherals that bus masters share, using round-robin, priority-based, or user-provided arbitration logic. Nios includes a royalty-free, perpetual-development license for designs placed in Altera devices. ASIC and applications-specific-standard-product licenses are also available.

ARM-based devices are also part of the Altera Excalibur embedded-processor programmable-logic-device family. These devices that feature an ARM922T processor core with 256 kbytes of SRAM; 128 kbytes of dual-port RAM; peripherals, including a UART, a timer, an SDRAM controller, and a memory interface; and a trace-debugger port.

Special instructions: Users can add as many as five instructions to the Nios ALU, providing single-cycle, combinatorial and multicycle, sequential operation. Each module supports a 32/16-bit A and B input, an 11-bit prefix, and direct access to external logic or memory. The development software automatically generates assembly and C-language macros.

Integrated peripherals: Nios includes several soft-core peripherals, including a UART, a timer, PIO, SPI, SDRAM, DMA, PWM, and IDE, in the development kit (i.e.). Additional development kits support Ethernet and on-chip debugging. Users may add any quantity and combination of these peripherals in their designs within the logic resources of the target device.

Development tools: The Nios development kit includes the Gnu compiler, an assembler, a debugger, and utilities. Optionally, users may purchase an Integrated Development Environment from VioSoft that supports the on-chip debug peripheral, hardware breakpoints, and address and data software trace. OS support includes Linux, ATI Nucleus, and Kros.

The Quartus II PLD-design software supports hardware development for the ARM-based Excalibur. The ARM ADS Lite development suite and Red Hat GnuPro tool suite support software development. ARM, Lauterbach, and Altera provide debugging support.

Analog Devices

THE ADUC812 ADUC816 AND ADUC824 microconverters have an 8051-instruction-set-compatible microcontroller core that integrates with multichannel SAR or sigma-delta ADCs. The ADuC812, an integrated 12-bit data-acquisition system, incorporates high-performance, self-calibrating, multichannel 12-bit, dual DACs and a programmable microcontroller on a single chip. The ADuC816 and ADuC824 smart-transducer front-ends incorporate dual high-resolution sigma-delta ADCs. The ADuC816 has dual 16-bit resolution converters, and the ADuC824 has both a 16-bit and a 24-bit ADC. The devices accept low-level signals directly from a transducer.

Power management: Static CPU operation, sleep and power-down modes for the converters allow power management for low-power applications.

Integrated peripherals: These devices include a watchdog timer, a power-supply monitor, ADC DMA functions, 32 programmable I/O lines, SPI, and a standard UART serial-port I/O. The ADuC812 also provides an on-chip temperature sensor, a 12-bit voltage-out DAC, dual excitation-current sources, a time-interval counter and a reference-detection circuit.

Development tools: The QuickStart Development System, incorporating an assembler, an in-circuit serial-port downloader, a serial port debugger, and analog-performance-analysis tools, support these devices. You can upgrade QuickStart to a full in-circuit, single-pin, nonintrusive, emulation system supporting assembly and C-Source debugging.

ARC Cores

THE ARCTANGENT-A4 IS A SYNTHESIZABLE, user-customizable processor core for embedded ASIC, SOC,

and FPGA integration. It is a 32-bit RISC architecture with optional DSP extensions. The basic processor requires as few as 8400 gates. Developers can configure and extend numerous features of the processor, including the instruction set, register files, I/O interfaces, interrupts, instruction/data caches, and condition codes. By customizing the processor, developers can create highly optimized, differentiated products while boosting performance, saving power, and cutting costs. Developers can customize the processor with the ARChitect configuration tool and add custom logic in HDL. The ARChitect tool generates RTL files and scripts for industry-standard logic-synthesis tools.

Power Management: Thanks to a low gate count, the ARCtangent-A4 processor consumes low power, but additional features allow further savings. Optional clock-gated domains and a sleep mode reduce power consumption to a trickle when particular parts of the processor are not in use.

Special instructions: ARC Cores offers a standard library of extension instructions, including DSP extensions. By using the ARChitect processor-configuration tool, developers can add the instructions they want, including saturating addition/subtraction, normalize (find first bit), minimum/maximum, two 32×32 -bit multipliers, and two 32-bit barrel-shifter/rotator blocks. DSP extensions include 16-bit, 24-bit, and dual 16-bit MAC (multiply-accumulate) instructions with XY data memories and special addressing modes.

Integrated peripherals: Using the ARChitect processor-configuration tool, developers can choose the peripherals they want to integrate with the ARCtangent-A4 processor core. Peripherals include 32-bit timers, as many as eight UARTs, a 10/100-Mbps Ethernet media-access controller, and a baseband controller for Bluetooth wireless technology. Adding these peripherals requires only a few mouse clicks with the ARChitect tool, which automatically generates the required RTL files and scripts for logic synthesis with industry-standard tools.

Development tools: The ARCform SOC development platform includes the ARChitect processor-configuration tool and other utilities for hardware development. Software development tools include the High C/C++ compiler, an assembler, a linker, a profiler, the SeeCode debugger, and an instruction-set simulator from MetaWare. Miscellaneous tools include the ARC Signal Visualization Tool for DSP development with Matlab and the Casseia cycle-accurate simulator.

ARM

ARM DESIGNS MICROPROCESSOR CORES and macrocells for its licensees in a variety of flavors with considerations for low power. The ARM7, ARM9, and ARM10 are base configurations and all implement the ARM instruction set, providing full software compatibility over a range of performance and prices. The cores support user and supervisor modes for controlling access; they handle interrupt-request, fast-interrupt-request, abort, and undefined-exception-processing modes. Cores with the S extension are synthesizable macrocells and allow configurability and tight coupling of the ARM processor core with SRAM, instruction and data caches, write buffer, and an AMBA (Advanced Microprocessor Bus Architecture) AHB (Advanced High-performance Bus) bus interface.

The ARM Thumb architectural extension is primarily a 16-bit subset of the 32-bit instruction set. The Thumb module, residing within the instruction pipeline, transparently decompresses the 16-bit instructions at execution back to 32-bit instructions without performance loss. The Thumb module adds about 6% to the core's die size but helps increase code density and overcome the added memory requirements that would come from using only 32-bit fixed-length instructions.

The SecurCore family of microprocessors features a new secure processor design and anticounterfeiting methodology. This methodology helps resist invasion at the hardware and software levels; physical tampering through reverse-engineering of the layout, power, or timing analysis; or directly probing the processor chip surface. A key feature for security-sensitive applications is the "one-way information flow" that permits developers to customize the core by adding a range of security features known only to the card issuer or developer.

Power management: All ARM processor cores are static designs that use gated clocks and transparent latches, clocking the logic only during an operation but not during a wait state. Using a unified cache enables lower clock speeds for the system bus and external memory than the processor, resulting in lower power consumption.

Special instructions: Cores with the E extension include signal-processing extensions to the ARM instruction set for those applications that would benefit from a mix of DSP and microcontroller

performance. The DSP extensions include single-cycle 16×16 - and 32×16 -bit MAC implementations and zero-overhead-saturation extensions of existing arithmetic instructions for use in the design of stable control loops and bit-exact algorithms. New instructions include the ability to load and store pairs of registers with a wider range of addressing modes and a new CLZ instruction that improves normalization in arithmetic operations and improves divide performance.

The ARM Jazelle architecture is another extension of the instruction set that enables ARM processors to execute Java byte code directly in hardware. Instruction extensions include set support for entering and exiting Java applications, real-time interrupt handling, and debugging support for mixed Java/ARM applications. From the programmers' point of view, the processor has a new mode in which it behaves like a Java machine. Once in Java state, the processor fetches and decodes Java byte codes and maintains the Java operand stack. The processor can switch easily, under operating system control, between Java state and ARM/Thumb state. Jazelle is completely compatible with the ARM interrupt and exception model.

Integrated peripherals: Peripheral options include DSP instruction-set extensions, on-chip debugging capability, JTAG interface, dual caches storing as much as 32 kbytes each, full MMU support, a vector floating-point coprocessor, and the AMBA-standard bus interface.

Development tools: ARM offers a variety of hardware- and software-development tools, including the ARMulator instruction set-set emulator and the ARM developer suite for software development. A range of third-party development tools and operating systems also support the ARM architecture.

The Jazelle Technology Pack is an add-on to the ARM Developer Suite that enables Java debugging over the ARM-standard debugging interface using the Java Debug Wire Protocol. The pack enables connectivity to the Jazelle technology target hardware via the Multi-ICE unit and allows you to debug the system software and Jazelle application using one connection.

Atmel

THE HIGH-PERFORMANCE, 8-BIT ATMEL AVR RISC microcontroller has 32 8-bit general purpose-registers that can function as accumulators and that the ALU can directly access. The AVR executes instructions in one clock cycle and was designed in collaboration with compiler vendors to provide tight C-language code density.

The Atmel AT89 family is a pin- and function-compatible MCS 51 flash-program-memory microcontroller supporting the industry standard 1-, 2- and 4-byte, 20-pin and the 4-, 8-, 20-, and 32-kbyte 40-pin package devices. In-system-programmable flash devices are also available.

Power management: The AVR supports four power-management modes. Idle mode stops only the CPU. Power-save mode stops the CPU and peripherals, but the real-time clock remains active. Power-down mode stops the CPU and all peripherals. ADC-noise-reduction mode halts the CPU to enable higher resolution measurements.

Special instructions: There are two-cycle 8×8 -bit-integer-multiply and fractional-multiplication instructions. There is zero flag propagation on add, subtract, and compare instructions that allows branches immediately after the instruction without updating the status register.

Integrated peripherals: The AVR architecture includes a UART; 8- and 16-bit timers; an eight-channel, 10-bit ADC with differential inputs and gain stage, an analog comparator, a brownout detector, SPI, I²C, and a watchdog timer.

Development tools: The AVR studio architecture simulator is the development environment for the STK 500 family of development kits and the ICE 10 and JTAG in-circuit-emulators. A variety of third-party vendors offers simulators, compilers, assemblers, in-circuit-emulators, and programmers supporting both families of devices.

Cybernetic Micro Systems

The general-purpose peripheral 8051-based P51 retains all 8052 features and addresses an (E)ISA/PC104 bus for connection to a host. Power-up resets the P51, and it remains reset while the host processor writes 8051 instructions directly into the P51's code RAM. These instructions begin executing when the host releases the P51 from reset. The ISA/PC104 interface enables the P51 to serve as a peripheral to almost any microprocessor, including an 8051.

Power management: The 4-kbyte, dual-port-RAM has eight equal segments and enables only the accessed segment at any given time.

Special instructions: In addition to all standard 8051 instructions, the P51 supports a 16-bit square-root instruction in the special-function-register file. The 8051 undefined operating code, 0A5h, is a breakpoint instruction for the P51 and allows the host to single-step the peripheral 8051.

Integrated peripherals: The P51 supports the standard 8051 timers, counters, UARTs, and interrupts.

Development tools: American Raisonance C-compilers and 8051-compatible cross-compilers support software development.

Cygnal Integrated Products

CYGNAL'S C8051FXXX DEVICES are integrated, 8-bit mixed-signal, SOC microcontrollers. The 8051 code-compatible CPU features a high-speed, pipelined architecture capable of 25-MIPS peak throughput. You can program the onboard, in-system-programmable flash memory in 512-byte sectors for both program storage and nonvolatile, user-data storage. The serial interfaces (SMBus/I²C, UART, SPI) are hardware implementations. The 5V-tolerant, high-current digital-I/O ports can easily drive LEDs. The onboard JTAG-based debugger uses no on-chip resources, providing nonintrusive, full-speed, in-circuit emulation using the production processor installed in the final application. This debugging system supports inspection and modification of memory and registers, setting breakpoints, watch points, single stepping, and run and halt commands.

Power management: User software manages the power to each chip subsystem. An ultra-low-power CPU core is completely static.

Special instructions: These devices are 100%-compatible with the standard 8051 instruction set and have no additional instructions.

Integrated peripherals: The 25-MIPS 8051-compatible CPU integrates an 8- or 12-bit, 100k-sample/sec ADC with a programmable-gain amplifier; two 12-bit DACs, a five-channel programmable counter array, three to five \times 16-bit timers, a watchdog timer, a missing-clock detector, a V_{DD} monitor, SPI, SMBus/I²C, UART, a temperature sensor, V_{REF}, two comparators, and a programmable oscillator.

Development tools: Every chip has built-in JTAG-debugging resources supporting single-stepping, memory inspection and modification, hardware breakpoints, and other functions. The \$99 to \$129 development kit from Cygnal includes a target board, a serial adapter, a power supply and cables, and the Cygnal IDE editor, assembler and debugger that can integrate seamlessly with 8051 C compilers.

Cypress MicroSystems

CYPRESS' 8-BIT MIXED-SIGNAL, CONFIGURABLE CY8C2XXXX family of devices are microcontrollers integrate 4, 8, or 16 kbytes of flash program memory, 128 or 256 bytes of SRAM, and 12 analog and eight digital programmable system-on-chip blocks. These blocks support thousands of peripheral combinations, replacing thousands of traditional, fixed-peripheral devices. Interconnected internally created peripherals permit the creation of hardware system flows (amplifier-to-filter-to-ADC). The pin-out is user-defined. The high-speed oscillator is 2½% accurate with no external components. The sleep/wake/watch oscillator can use a crystal if time-keeping is necessary, and you can use it to phase-lock-loop the high-speed oscillator for crystal accuracy.

Power management: These devices run at 3.3 or 5V and have internal pump-control circuitry that, with three external components, allows operation from single battery sources to power as low as 1.2V (excludes the CY8C25122).

Special instructions: These devices support hardware multiply and multiply-accumulate instructions.

Integrated peripherals: The devices have fixed watchdog, low-voltage-detection, and sleep-timer peripherals. Users define the timers, counters, PWMs, serial I/Os, UARTs, ADCs, DACs, filters, and amplifiers using hardware peripheral-building blocks. Other available functions include hardware CRC generation and pseudorandom-sequence generation.

Development tools: A full-software windowed interface provides assembly-based tools with an

optional C compiler. A device editor selects and interconnects the desired peripherals. A \$150 ICE provides complex breakpoints, real-time trace, external triggers, and break-anywhere features.

Fujitsu Microelectronics

FUJITSU SUPPORTS A RANGE of applications with 8-, 16-, and 32-bit microcontroller families. The F2MC 8L microcontroller family offers a range of peripheral functions, memory sizes, and options. More than 30 device series are available, incorporating features such as A/D and D/A converters, LCD and VFD drivers, I²C and UART interfaces, and ac and stepper-motor drivers. Each series offers 4 to 60 kbytes of mask ROM and 128 bytes to 18 kbytes of SRAM. All series have a choice of mask-ROM sizes and at least one member with a one-time programmable EPROM. The architecture includes an 8-bit CPU core; two 16-bit accumulators; seven dedicated 16-bit registers; and 32 register banks, each comprising eight 8-bit registers. Typical applications include metering, motor control, domestic appliances, automotive, and feature phones. This series of microcontrollers offers a large memory space that contains an I/O area, a RAM area, a ROM area, an external area, general-purpose registers, and a vector table. In addition to 10 addressing modes, the series has special instructions for jump, move, multiplication, division, and subroutine calls. It also has bit-manipulation instructions for bit set and clear.

Available in three variants, Fujitsu's F2MC16L, LX and F series 16-bit CPU cores feature bit, nibble, byte, word and long-word data types, and 23 addressing modes. The instruction set supports a 16-Mbyte address range using bank- or linear-addressing modes. On-chip registers, such as user and system stack pointers, together with their supporting instructions, provide advanced support to real-time operating systems. All of the F²MC-16LX series and one of the F²MC16L series offer at least one device that has flash ROM as the user-programmable memory. Available block sizes are 64, 128, 256, or 384 kbytes divided into separately erasable and protectable sectors supporting a minimum of 10,000 erase cycles. The 5 and 3V devices require no second programming voltage. Special instructions include support for enhanced high-level language and multitasking, enhanced pointer indirection, and barrel-shift operations.

Fujitsu's FR series RISC architecture is a new generation 32-bit microprocessor core for control systems in high-performance automotive, consumer, and telecomm applications. Optimized for embedded applications with one-cycle instruction execution and 16-bit instructions that derive maximum performance from low cost, half-word external memory and instruction-cache widths or by supporting double instruction fetches each bus cycle. The CPU employs a five-stage pipeline and 32×32-bit multiplier with a barrel shifter and bit-search unit that finds the first zero, one, or change in a data word. The general-purpose user-logic bus, provides access to the on-chip flash ROM and CAN (controller-area-network) interfaces.

Power management: Power management consists of sleep, stop, and watch modes. These standby modes reduce the power consumption by stopping operation of CPU and peripheral functions. The main and subclock modes support changing between sleep, stop, and watch modes.

Integrated peripherals: All of the device families include A/D and D/A converters, a UART, and an LCD controller. The F2MC 8L series includes a VFD driver, a DTMF generator, inverter-motor control, and USB support. The F2MC 16L/LX/F series includes stepper-motor control, an ac/dc-motor-control macro, real-time control, CAN controllers, and an FL display driver. The FR series includes a DRAM interface, cache memory, a DMA controller, as many as three CAN controllers, a stepper-motor controller, a bit-search module, a 16-bit reload timer, and interrupt controllers.

Development tools: The Windows-based Softune Workbench integrated development environment for developing software includes a C/C++ compiler, a development manager, a simulator debugger, an emulator debugger, and a monitor debugger. In-circuit emulators, programmer kits, and evaluation boards are available.

Hitachi Semiconductor (America)

THE SH-2 AND SH-3 SERIES of RISC-microcontroller devices employ a fetch, decode, execute, memory-access, and write-back-to-register pipeline. The SuperH family has devices with single-cycle mask ROM, OTP, flash memory with maximum densities of 512 kbytes and 32 kbytes of RAM. SuperH processors use a 16-bit instruction word to achieve compact code. The instruction width limits the number of

basic operation codes, handles only 16 general registers, and addresses only two operands. Additionally, only 12 bits are available for an immediate offset; jumps with immediate data must be in 2048-byte hops. However, the SH-3 supports far-relative branches to support position-independent code. Although these restrictions lead to more instructions per task, the overall result is significantly smaller code.

Power management: Sleep mode discontinues CPU processing but keeps peripherals active. Standby stops everything but maintains register and cache contents. Software can adjust the clock rate during program operation. The SH-3's unified-cache, low-power design dissipates 100 mW during operation.

Special instructions: A 32×32-bit multiply-accumulate instruction supports DSP functions.

Integrated peripherals: The SH-2 features a two-channel, 16-bit compare-match timer; a 10-bit A/D converter; serial I/O; a multiplier; and a watchdog timer. The controllers also have a data-transfer controller with an 8-bit external bus, an interrupt controller, a user-break controller, and a clock-pulse generator with a built-in multiplication PLL. The SH-3 includes an MMU and various on-chip modules, such as IrDA, SmartCard, a real-time clock, a serial-communication interface, a color-LCD controller, a USB-host controller, glueless connection to SDRAM, JTAG, real-time trace, and power-down.

Development tools: Hardware- and software-support products are available from Hitachi and third-party vendors. The SH7047F chip incorporates the Hitachi debugging interface and advanced user-debugger on-chip debugging functions, enabling simple emulation via the Hitachi E10A PC card-emulator development tool. The SH-3 offers on-chip debugging functions, the Hitachi user debug interface and advanced user debugger that allow real-time emulation at the processor's 160-MHz maximum operating frequency during system evaluation using the Hitachi E10A PC-card emulator-development tool.

Improv Systems Inc

IMPROV SYSTEM'S JAZZ Processor uses a VLIW (very-long-instruction-word) architecture comprising a mix of heterogeneously configured task engines, on-chip data and instruction memory, I/O modules, and the QBus global bus for on-chip task and control communications among processors. System designers can tailor each task engine to match the computational needs of specific tasks by adding or removing execution units. A task engine contains as many as 16 single-cycle integer-computation units from a collection of functional blocks that include ALUs, multiply-accumulate units, shifters, counters, and application-specific units. Designers can create task engines for 32- or 16-bit datapaths and can also add custom units and instructions using the Jazz PSA Composer. Memory-interface units connect the processor to shared- and private-memory blocks and I/O modules. Each memory unit has a 32-bit datapath and can address 64 kbytes of data memory as word, half-word, and byte-wide read/write operations.

Power management: The processor supports idle, sleep, static-state held, and glitch-free clocking, resulting in a 98% clock shutdown.

Special instructions: The user can incorporate specialized gate-level descriptions within the datapath of the Jazz programmable processor and extend the programming environment to support these as special instructions.

Integrated peripherals: The Jazz Processor can act as an integrated peripheral to other host-oriented microprocessor solutions, such as ARM and MIPS, extending their functions for application-specific requirements.

Development tools: The Jazz PSA Tool Suite provides an integrated development environment with advanced debugging, compilation, and analysis capabilities to support production-code development for Jazz PSA Platforms. A compilation system manages applicationwide partitioning and allocation, coupled with advanced task optimization and code generation.

Infineon Technologies

THE UNIFIED MICROCOMPUTER/DSP CORETRICORE architecture operates as a single multitasking engine with fast context switching. Execution of interrupts begin at just four cycles. The TriCore-based TC-1MP microprocessor is available as a hard-core and fully synthesizable macro for system-on-chip integration. Combining a classic load/store RISC architecture with Harvard math capability, the superscalar TriCore

core has three four-stage pipelines, enabling simultaneous execution of as many as three instructions and a maximum rate of execution of seven operations in one clock cycle. You can freely intermix 16- and 32-bit instructions without degrading code-execution efficiency. Applications for the core include servo control; audio-domain DSP, such as speech processing; data communications; modems; automotive systems; and portable applications, such as wireless phones and Internet appliances.

The TC1775 is part of TriCore-based Audio family for real-time control in an environment requiring digital-signal analysis, such as automotive power-train systems. The TC1775 implements a three-layer architecture. The application layer runs complex, real-time control algorithms. The peripheral-control layer relies on an independent 32-bit processor to act as the interface between the application and the physical layers. The physical/peripheral-interface layer supports I/O functions, including both analog- and digital-signal acquisition and output-signal generation. TC1775 supports DSP capabilities, such as zero-overhead looping, bit-reverse addressing, fractional arithmetic, and automatic saturation. These features enable you to implement tasks such as knock detection, ion-current sensing, and other engine-specific features with more software and less external hardware.

The TriCore-based, general-purpose TC111B industrial microcontroller has an extensive set of on-chip communication peripherals supporting high-integration applications, such as industrial communication devices, or a slot CPU in a PC. The external bus unit complies with the PC100 specification and integrates PCI and Ethernet on-chip. The 1.5-Mbyte embedded DRAM lets you implement single-chip designs using sophisticated real-time operating systems.

The C166 family offers microcontrollers with varying levels of performance, peripheral support, and programmability, supporting integration in wireless-baseband controllers. All C166 devices execute the same basic instruction set and are based on a cross-licensed and co-developed architecture with STMicroelectronics.

Power management: Power modes include stop and step down of the CPU-, component-, and peripheral-clock speeds. You can configure all on-chip units for power-saving modes.

Special instructions: The TriCore architecture combines microcontroller and DSP functions, such as bit-manipulation capabilities, in one instruction set. The TC-1MP supports one to four coprocessors, tightly coupled to core, to implement custom or application-specific instructions.

Integrated peripherals: The devices integrate peripherals via the flexible peripheral-interconnect bus and the peripheral-control processor. The 32-bit peripheral controller manages intelligent-DMA operations, adds 256 interrupts, and can operate in parallel with the core. Some devices provide high-speed-synchronous and asynchronous/synchronous serial interfaces, PC100, PCI V2.2, fast Ethernet, CAN (controller-area network), USB, ADCs, IrDA, real-time clock, multimedia-card interface, JTAG, and multicore debugging.

Development tools: The TriBoard evaluation board includes full processor and system memory. Softcore deliverables include synthesizable RTL, complete scripts, a sample testbench, and documentation. Dozens of third-party providers offer development environments, ICEs, and RTOSs. The Digital Applications Virtual Engineer software-code generator and software-development kit supports all C166 processors and direct interfaces to third-party tools, extensive configuration, and what-if-scenario analysis.

Integrated Device Technology (IDT)

THE IDT FAMILY OF PROCESSORS integrates a 32-bit MIPS core with peripherals, such as an SDRAM controller, a general-purpose memory/IO controller, and a PCI bridge. These processors target communications, consumer, and industrial applications. The RC32355 includes four communication-specific interfaces that make it suitable for home- and small-office customer-premises-equipment-gateway systems. EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium) benchmarks for these devices operating at 150 MHz are 1.8 for Telemark and 1.6 Netmark.

Power management: You can save power by halting the CPU during periods of inactivity, and you can restart the CPU by asserting an interrupt.

Integrated peripherals: The RC323xx processors include a PCI Version 2.1-compatible bridge, an SDRAM controller, a general-memory/IO controller, an SPI interface, and a serial port. The RC32355 adds support for 10/100-Mbps Ethernet, a USB Version 1.1-compatible interface, a 25-Mbps segmentation-and-reassembly interface, an 8-Mbps time-division-multiplexed module, and an I²C inter-

face.

Development tools: Compiler and development tool chains are available from Algorithmics, Green Hills, and Metaware. Accelerated Technology, Red Hat, and Wind River provide and support the Nucleus, Linux, eCOS, and VxWorks real-time operating systems. In-circuit emulators are available from Corelis, Embedded Performance, Lauterbach, and Wind River. Intoto is a source for Internet Protocol-security software. Jungo and Wind River offer application-level code for home gateways.

Intel Corp

Intel implemented the XScale microarchitecture in the 80200, a 32-bit superpipelined RISC processor that complies with the ARM Version 5TE instruction set. The architecture features dynamic voltage management that permits scaling of the processor voltage and frequency, enabling longer battery life for wireless- and handheld-multimedia devices and increased device density for Internet-infrastructure applications by throttling power dissipation and managing thermal output. The 80200 processor includes a 40-bit multiply-accumulate unit that supports 16-bit single-instruction, multiple-data and DSP extensions. The companion 80312 I/O chip provides a 64-bit, 66-MHz PCI-to-PCI bridge, a memory controller for as much as 512 Mbytes of 64-bit SDRAM, three DMA channels and an I²C-bus interface.

The 80486 family of 32-bit processors offer multiprocessor-system support, on-chip integration of Level I unified code and data cache, a memory-management unit with paging, a floating-point unit, and clock speed-multiplying that allows the processor to operate at frequencies higher than the external memory bus. The 80386 family of 32-bit microprocessors support embedded pc-board, industrial-control systems, medical instrumentation, and applications that use MS-DOS and Windows software. The integrated memory-management and -protection architecture includes address-translation registers, multitasking hardware, and a protection mechanism to support operating systems. Code compatibility from 80386 to 80486 processors supports device migration for increased embedded-system performance.

The i960 architecture family comprises 32-bit embedded RISC processors that are object-code-compatible across all six major series that span low-power devices to superscalar devices. These processors target page-printer, data-storage-management, industrial-control, telecommunications, and imaging applications. The 16-bit, embedded MCS96/296 microcontroller families target event processing, high-speed I/O, and motor control. The MCS96's register-based architecture reduces accumulator bottlenecks and enables fast context switching, supporting bit, byte, word, and 32-bit operations. The 8-bit MCS51/251 microcontroller family targets event control for applications such as traffic-control equipment, input devices, and computer networking. The MCS251 is a descendent of the MCS51 architecture, featuring 18-bit linear addressing and an extended instruction set for 16- and 32-bit arithmetic and logic instructions.

Power management: Most devices support modes for reducing power consumption. Idle mode discontinues CPU processing but leaves the clock, timer, and serial-peripheral and communications-interface systems enabled. Power-down stops the clock and internal processing. Both modes maintain RAM and enable interrupts to wake the CPU. Most peripherals support selective disabling. XScale microarchitecture devices with dynamic voltage management allow scaling of the clock frequency and voltage to adjust performance and power consumption.

Special instructions: XScale processors extend the ARM Version 5 instruction architecture and include DSP extensions. The MCS296 instructions include multiply-accumulate, indirect-auto increment addressing, block data move, and table-indexed jump instructions. The MCS-51 includes bit-manipulation instructions, including AND or OR with a carry bit for a 16-byte area of RAM and some special-function registers. The MCS-251 extends the MCS-51 instruction set by 128 instructions covering 16- and 32-bit arithmetic and logic instructions.

Integrated peripherals: Intel processors support a combination of features that can include DMA, I²C, high-speed I/O, PWM, A/D converters, a PCI interface, a watchdog timer, asynchronous and synchronous serial I/O, parallel I/O, JTAG-debugging support, and a floating-point unit.

Development tools: A range of third-party development-tool vendors support Intel's processors with products ranging from development-tool suites to in-circuit emulators and programmers. Debugging features for each device can include built-in self-test, on-circuit emulation, JTAG debugging, and direct access to the page-translation cache.