

Lexra

INTRODUCED APRIL 2001, Lexra's 420-MHz, 32-bit LX4380 RISC core is optimized for 0.13-micron processes. Designers can incorporate as much as 64 kbytes of onboard cache to benefit from a new background-move instruction that performs a DMA transfer to or from cache while the LX4380 concurrently processes data. The new seven-stage pipeline and partitioning of the CPU design deliver high performance. All critical paths are in the same Verilog module, avoiding the timing problems that occur when critical paths cross Verilog-module boundaries.

The 32-bit LX4189 RISC core is optimized for 0.15-micron silicon processes and targets communications applications in which performance is critical. The extra stage in the six-stage-pipeline design performs instruction-memory access that enables the processor to access more memory and keep the clock frequency high for high throughput. Clock speeds can reach 266 MHz for the worst-case process at industrial temperature without using full custom-circuit designs.

Power management: Inhibiting the clock to inactive blocks of logic, using a register file that clocks data only when the data changes, optimizing the clock/buffer trees in the CPU, and using clock-gated-enable flips-flops minimize the power consumption of the devices.

Special instructions: The LX4380's background-move instruction is a DMA transfer to and from local CPU memory of any length up to the size of data memory. The CPU executes without stalls until the data transfer completes. A 64-bit twin-register-load operation transfers data between data memory and the general register file. The LX4380 does not support unaligned loads and stores in hardware or software.

Integrated peripherals: Linux supports LX4380's new optional MIPS R3000-style MMU.

Development tools: Software-development and debugging tools are available from Green Hills Software, Accelerated Technology, California Express Logic, Advanced Software Tools, and Embedded Performance.

Microchip Technology Inc

THE EIGHT-PIN PICMICRO FAMILY of products packs Microchip's RISC-based 8-bit processor architecture into eight-pin DIP and SOIC packages and offer a variety of program-memory options, such as flash, OTP, and ROM for small-footprint applications. Developers can choose from pure-digital products to devices with ADCs, onboard EEPROM, PWM module, programmable low-voltage detect and brownout reset. The PIC12C5x family features a 12-bit instruction set, low operating voltage of 2.5 volts, internal oscillator and onboard EEPROM data memory. Migrating between products or even into higher pin count devices is supported because all the devices are code and pin compatible, enabling designers to re-use existing code.

The PIC16Cx family provides completely upward-compatible devices in 18- to 44-pin packages with a range of peripheral-integration options. This family features a 14-bit instruction set, four to eight channels of 8/10-bit A/D converters, interrupt-handling capability, various serial-interface capabilities, capture/compare/PWM, brownout detection and an eight-level stack. PIC16FX devices with flash program memory allow low-voltage reprogramming. The PIC16CX/FX family targets applications ranging from security and remote sensors to appliance-motor control and high-speed-automotive applications.

The PIC18x family provides devices that are upwardly socket- and software- compatible with PIC16x devices. This family features various serial-interface capabilities, capture/compare/PWM, 8/16-bit timers, a parallel slave port, a 10-bit A/D converter, a watchdog timer, power-on reset and CAN 2.0B. Most PIC18x devices provide flash program memory of 8k to 64k words and data RAM of 512 bytes to 4 kbytes that operates 2 to 5.5V and at dc to 40 MHz.

Power management: The low-power sleep mode reduces power consumption to only transistor leakage to maintain RAM and register contents while stopping all clocks. Devices operate at 32 kHz to save power.

Special instructions: PICmicro bit-manipulation instructions are bit set, clear, and test. Math functions include add, subtract, increment and decrement. The PIC16X family has a decrement-and-skip-on-zero instruction.

Integrated peripherals: Eight-pin devices provide in-circuit serial programming of program mem-

ory for EPROM/OTP, an internal 4-MHz oscillator with programmable calibration, a watchdog timer with its own on-chip RC oscillator, and programmable code protection. Devices may include an USART/SCI, an 8-bit parallel slave port, brownout detection, serial-peripheral interface, I²C, 8/10-bit A/D converters, and capture/compare/PWM modules.

Development tools: Microchip offers the MPLAB integrated development environment, a C compiler, a macro assembler, emulators, simulators, in-circuit emulators and debuggers, fuzzy-logic-development software, and modular device programmers. More than 110 third-party developers offer development systems for the PICmicro architecture.

Mitsubishi Electric & Electronics USA

THE M32R/E FAMILY INTEGRATES a RISC CPU, 32×16-bit multiply-accumulate (MAC) unit, and a multitude of on-chip peripherals. The CPU executes most instructions in one clock cycle using an instruction fetch, decode, execute, memory access, and write-back. The decoding stage dispatches instructions in order, and the remaining stages execute them out of order to hide memory-access latency. The MAC unit contains a single-cycle, 32×16-bit multiplier and a 56-bit accumulator. The CPU has an instruction queue of two 32-bit entries. The memory maps directly to the address space and has memory modes for internal instructions and data, for internal and external instructions, and for external memory only. If a memory miss occurs, the CPU fetches one 32-bit data line in five cycles.

The three-stage-pipeline M16C CPU takes advantage of both accumulator- and register-based architectures. The instruction formats are zero, short, quick, and general. Programs that use 8-bit registers use the zero and short formats. The quick instruction format is useful for creating frequently used subroutines with minimal bytes. The general instruction format allows the transfer of data between any two registers within the CPU or the 1-Mbyte address space that you can address linearly or as four chip-select areas. Other features of the M16C include a 4-byte prefetch queue for pipelining, a 16×16-bit multiplier, and a user-selectable 8- or 16-bit-wide data bus. Each of the two register banks comprises six 16-bit general-purpose registers and one frame-base register. The frame-base register helps manage the stack for C functions with local variables. You can use two registers as four 8-bit registers and two others as address registers. An additional register bank contains a static base register, a dedicated interrupt-stack pointer, and a stack pointer for user programs.

The 740 family comprises hundreds of devices built around an 8-bit, accumulator based CISC architecture. The 7600 series includes an integrated DMA interface, a software-programmable slow-external-memory interface, and a hold function for use when more than one device needs control of the external address and data bus. Peripherals are memory-mapped into the special-function-register area of RAM. The 38000 series has a 64-kbyte linear-address space with as much as 60 kbytes of integrated memory. A memory-expansion mode enables external memory through an external 16-bit address bus and 8-bit data bus.

Power management: Each device supports disabling each peripheral, the stop instruction that stops the clock to the entire device, and the wait instruction that stops the clock to the CPU. Interrupts such as key-on wake-up can make the device exit these low-power modes. Most devices also support a 32-kHz real-time-clock input, allowing the microcontroller to continue executing code after stopping the fast main clock.

Special instructions: The M32R/E family supports 32×16- and 16×16-bit multiply-accumulate operations and performs data rounding in the accumulator and block moves. The M16C can perform 1-, 4-, 8-, and 16-bit operations and includes a repeat-multiply-and-accumulate instruction that uses the hardware-multiplier circuit and can perform a 16×16-bit multiply in five cycles. Graphics processing can use an instruction, which matches the remainder sign to that of the divisor. The 740 family offers bit manipulation, memory-to-memory data transfer, and data transfers between the index registers and accumulator.

Integrated peripherals: The M32R/E family integrates as many as six serial-I/O channels and a 10-channel DMA controller, in which each channel can transfer as much as 256 bytes at once at up to 13.3 Mbytes/sec using cycle-stealing, single-transfer, continuous-burst-transfer or cycle-stealing, continuous-transfer mode. Other M32R/E functions include timers, a real-time debugger, JTAG, a wait controller, an A/D converter, and a CAN controller.

Some of the functions available on M16C devices include a 10-bit A/D converter with sample-and-

hold circuitry, a D/A converter, an I²C-bus interface, as many as four DMA channels, a watchdog timer, as many as five full-duplex UARTs, and a three-phase inverter controller. The M16C family supports a masked-ROM program-correction function that uses an address-match interrupt scheme to allow designers to correct two faulty mask-ROM program areas with an external EEPROM. These microcontrollers also have 16-bit CRC circuitry that uses the CRC-CCITT (X¹⁶+X¹²+X⁵+1) polynomial with either of the chip's UARTs. Some microcontrollers have LCD, CAN, USB, keyboard, and DRAM controllers.

The 38000 and 7600 series devices application-specific microcontrollers incorporate some combination of peripherals that include a successive-approximation A/D converter, a DAC, an LCD controller, a PWM, a watchdog timer, a USART, a UART, serial I/O, timers, a comparator, ROM, RAM, EPROM, and LED drivers. You can group these devices into on-screen-displays/TVs, keyboard controllers, LCD controllers, low-pin-count Slim740s, and general-purpose microcontrollers. The 7600 series also supports USB, CAN, IrDA, DMA, sigma-delta ADCs, other A/D converters, PLL, and low-voltage detector.

Development tools: Wind River supplies the Tornado integrated development environment as well as the pRISM+ integrated development environment for the pSOSystem real-time operating system. Red Hat supplies the GnuPro software-development tool suite, including C and C++ compilers and debuggers. Diab Data supplies a C and C++ compiler. Mitsubishi Electric also supplies a C compiler, an emulator, and an evaluation board.

Motorola

THE MPC7XXX SERIES PROCESSORS are 32-bit implementations of the PowerPC RISC architecture and Motorola's 128-bit AltiVec technology targeting network-control and -storage, telecommunications, high-end-embedded, scientific, and computing applications. Low-power versions of these devices are available. Software compatibility between PowerPC 603e, 750, and 7xxx processors protects software investment using the AltiVec technology, which targets high-bandwidth, data-processing, and algorithmic-intensive computations, such as MPEG 2 encoding; continuous-speech recognition; and real-time, high-resolution, 3-D memory for 3-D graphics. The seven to 11 independent execution units allow the devices to issue as many as two or three instructions and one branch instruction per clock cycle. Separate memory-management units for instructions and data support 4 Pbytes of virtual memory and 4 Gbytes of physical memory. The MPX-bus architecture with a 64-bit data bus and a 32-bit address bus supports burst, split, and pipelined transactions, data streaming, out-of-order transactions, and data intervention in SMP systems. The interface provides snooping for data cache-coherency and implements the MERSI (modified, exclusive, reserved, shared, invalid) coherency protocol for multiprocessing in hardware allowing access to system memory for additional caching bus masters.

The MPC8245 is highly integrated PowerPC device, reducing chip count from five discrete chips to one, targeting systems using PCI interfaces in networking infrastructure, telecommunications, control processing for network storage, and image-display systems. The 603e microprocessor is a low-power implementation of the PowerPC RISC architecture.

PowerQuicc devices integrate the embedded PowerPC core with a communications-processor module delivering support for protocols including Ethernet, Fast Ethernet, ATM, HDLC, USB, and PCMCIA. PowerQuicc processors target small-office home-office applications, remote-access routers, digital-subscriber-line-access multiplexers, access concentrators, LAN/WAN/central-office switching, integrated access devices, residential gateways, and DSL/cable modems. The communications-processor module handles Layer 2 communications protocol, allowing the PowerPC core to handle higher level software tasks.

The 16-bit 68HC16 family targets expanded memory applications that require high-performance serial communications and basic analog functions with the 68HC16 Z series. The 68HC16 Y series offers single-chip devices with flash or ROM, a time-processor unit, SCI, SPI, and an ADC. The 68HC16 X and R series addresses lower cost and pin count single-chip devices with flash, serial, and analog capabilities. The 16-bit 68HC12 family comprises devices such as the 68HC12 A series that features as much as 5 Mbytes of external addressing capability, PLL, and dual-SCI modules. The 68HC12 B series includes flash EEPROM and byte-erasable EEPROM on-chip. All devices in this family incorporate a byte-data-link-control or controller-area-network module. The 68HC12 D series incorporates dual-SCI modules, a controller-area-network module, 10-bit A/D converters, program and data memory using

both flash and byte-erasable EEPROM, PLL, and keyboard interrupts. The 16-bit 68HC11 family comprises six major series of microcontrollers, each offering many related devices ranging in performance, memory, and peripheral support. Some, such as the 68HC11D3, target applications in which 8-bit performance requires fewer peripherals and less memory. The 68HC11 E family offers flexible I/O capabilities, and the 68HC11 K family offer high speed, a memory-management unit, and PWMs.

The 8-bit 68HC08 family incorporates an SAE J1850 Class B-compliant serial-communication multiplex-bus controller and targets automobiles in which multiple microcontrollers communicate over a single- or dual-wire bus. The 8-bit 68HC05 family offers general-purpose devices that feature many memory options, on-chip asynchronous serial communications with software-selectable baud rates as high as 250 Kbps, and SPI for driving off-chip displays and peripherals. Each family device include a powerful 16-bit, free-running, programmable counter and input-waveform-measurement and output-waveform generation.

Power Management: PowerPC processors feature user-programmable nap, doze with bus snoop, and sleep modes, which progressively reduce the power the processor draws. The PowerPC 603e selectively activates functional units as needed while unused functional units automatically enter a low-power state without affecting performance, software execution, or eternal hardware. The PowerQuicc family provides automatic dynamic-power reduction when internal functional units are idle. The 68HCxx devices feature wait and stop modes for reducing power consumption.

Special instructions: The 68HC16 family have a multiply-accumulate instruction. The 68HC12 family support instructions for fuzzy-logic operations.

Integrated peripherals: MPC8245 devices include an integrated PCI bus, an SDRAM controller, and a clock generator. PowerQuicc devices support OC-3 ATM, 10/100 Ethernet, and 68HCxx devices support a serial-peripheral interface.

Development tools: Motorola and more than 65 independent suppliers provide development-tool support for Motorola devices with emulators, logic analyzers, programmers, evaluation boards, simulators, C compilers, real-time operating systems, assemblers, and debuggers.

National Semiconductor

THE NATIONAL SEMICONDUCTOR GEODE family of processors target information appliances such as thin clients, interactive set-top boxes, personal access devices, and WebPAD devices. The processor's x86 architecture supports popular software plug-in modules for Internet access.

Power management: Power management includes support for the Advanced Power Management and Advanced Configuration and Power Interface standards for legacy and Windows power management. Hardware-and software-controlled modes include active-idle in which only the core stops, standby in which the core and all integrated functions halt, and sleep in which all devices and the external clocks stop.

Special instructions: The device support the MMX instruction set extension for multimedia acceleration.

Integrated peripherals: Geode processors are six-stage-pipelined, -integer units that include a integrated floating-point unit, a 16-kbyte unified L1 cache, and a memory-management unit that adheres to standard paging mechanisms and re-entrant system-management mode enhanced for National Semiconductor's virtual system architecture technology.

NEC Electronics

NEC BASED THE VR5000 SERIES DEVICES on the 64-bit MIPS R5xxx processor core that features a symmetric dual-issue pipeline with six independent execution units that execute any combination of arithmetic-logic unit, floating-point, or rotate instructions, while 32-kbyte instruction and data caches implement cache-line locking to cache critical code and data. To enable each pipeline handle integer and floating-point operations, the floating-point mantissa and exponent are split between the integer portion of the pipe and a separate 12-bit ALU. The VR5500 implements a two-way, out-of-order pipeline that selects and dispatches two of the 16 fetched instructions out of order to one of the appropriate integer units, floating-point units, the branch-prediction unit, or the load/store unit. The VR4310 is the highest performing member of the VR4300 series of microprocessors. It targets applications for portable systems needing 64-bit performance. The VR5432 of the VR5000 series is the growth path for this device.

VR4100 series devices implement the MIPS III instruction set and include integrated peripherals that target a range of performance requirements for low-power, portable applications.

The V850 family of 32-bit RISC microcontrollers and ASIC cores have DSP features, such as multiply accumulate, and peripheral options targeting applications in consumer electronics that can benefit from high integration and low power consumption. The V850 offers various on-chip memory configurations integrated with a suite of standard peripherals, analog converters, high-speed serial interfaces, and I/O ports. The devices have 32 general-purpose registers that can act as a soft register bank with two register sets when you use them with a compiler that can map general-purpose registers. EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium) scores for a 50-MHz V850E are 10.9 for automotive applications, 2.9 for consumer applications, 0.5 for networking applications, 28.7 for office-automation applications, and 0.6 for telecomm applications. EEMBC scores for a 143-MHz V832 are 21.5, 5.3, 1.2, 54.4, and 1.3 for auto, consumer, networking, office-automation, and telecomm applications, respectively.

The 8-bit K0 family is divided into integrated general-purpose devices and devices for LCD, fluorescent-indicator panel, and application-specific-standard-product designs. Each K0 device offers memory as large as 60 kbytes of ROM. The 16-bit K4 family offers memory-mapped peripherals and as much as 128 kbytes of ROM and 4 bytes of RAM. These devices target wireless-communication devices, point-of-sale systems, industrial-control systems, and office-automation products. Context-switching features and macro services from the peripheral-management unit allow rapid interrupt processing with little or no CPU intervention. The KO/KOS and K4 families have the same architecture that allows designers to use a common design platform throughout the K Series. The instruction set, memory map, peripherals, and other onboard support circuitry are common to all three families.

Power management: Each device family supports various power-reduction modes, including clocking the processor and peripherals at lower frequencies; stopping specific peripherals; stopping the core while leaving the peripherals running; and stopping the oscillator, core, and peripherals. These modes maintain the registers and the memory. Some devices can wake up the processor without waiting for oscillator and PLL stabilization.

Special instructions: VR5000 series devices implement the MIPS IV instruction set plus integer and other register-based multiply variations for fast-DSP support, integer-rotate instructions for fast 32/64-bit string operations, leading-one/zero count, packed-data-vector operations, and cache-line-locking instructions. The VR4310 implements the MIPS III instruction set. VR4100 series devices implement the MIPS III and MIPS 16 instruction sets and include instructions for single-cycle multiply-accumulate. V850 devices support a two-cycle multiply-accumulate instruction, single-cycle byte-swapping operations for endian translation of data structures, a software-trap instruction, and instructions to assist in C procedure calls for pushing and popping multiple registers' code in the prologue and epilogue sections. The devices can also perform saturate operations that store maximum values of additions that result in overflow. The K family supports instructions for hardware multiplication and bit/nibble manipulation.

Integrated peripherals: VR5000 devices have a 32- and 64-bit data-interchange ability intended for use with system controllers, such as the 32-bit NEC VRC5477 and the 64-bit Marvell/Galileo 64120A. The VRC4375 system controller is a companion chip for VR4300 series devices. The VR4181's integrated peripherals include an LCD controller, CompactFlash, a power-management unit, an interrupt-control unit, timers, a real-time clock, a 16550-compatible serial interface, IrDA 1.0, a keyboard and touch-panel controller, USB, an A/D converter, and a D/A converter. The rest of the VR4100 series devices support 32-bit PCI Version 2.1, fast IrDA 1.1; an interrupt controller; a real-time clock; a 16550-compatible serial interface; serial debugging interfaces; and a synchronous, three-line, serial clock. Additional peripheral support is available from the VC4173 system controller for USB, a PC-card controller, an ac link, a 12-bit analog/digital audio controller, and a touch-panel and keyboard controller. V850 devices include a combination of UARTs, a 10-bit A/D converter, an 8-bit D/A converter, an extended-data-out SDRAM controller, a synchronous-flash controller, DMA controllers, a CAN interface, and a timer for inverter control that can generate six channels of PWM.

Development tools: NEC supplies tools for a quick start on development efforts. Development resources for the VR series devices include compilers' development environments' and RTOSs, such as Linux, VxWorks, and Windows CE. The SS-V850 emulation system enables designers to perform real-time emulation and includes onboard flash-programming capability. The system includes the Green

Hills Multi integrated development environment and a Red Hat Gnu C compiler. Other evaluation boards are available from NEC and third-party vendors. Accelerated Technology, Green Hills Software, NEC, Integrated Systems, and Wind River Systems provide RTOSs. NEC works jointly with Cadence and Mentor Graphics to provide cosimulation tools for the V850 Series embedded-core/ASIC development. NEC's OpenCAD environment supports these tools. An emulator that includes a flash programmer and a parallel interface to a host PC supports development for the K family. Software-development tools include an integrated debugger, a relocatable assembler, an optimized C compiler, and a system simulator.

NetSilicon

THE ARM7TDMI-BASED NET+WORKS products from NetSilicon target Internet-telephony, building-access and -control, wireless-base-station, retail-point-of-sale, office-appliance, and handheld-computing applications. When you couple the Net+Works products with a physical interface and ROM, the products offer the hardware and networking software necessary to add Ethernet/Internet connectivity to electronic-product designs. Net+Works also includes software and firmware for an integrated and tested embedded-networking product.

Integrated peripherals: The Net+Works on-chip peripherals include a 10/100 Ethernet media-access controller; an integrated cache; a DMA controller; serial interfaces; IEEE 1284 ports; and an embedded-network interface with a shared, 64-kbyte RAM interface for dual-processor applications.

Oki Semiconductor

A 32-BIT ARM7TDMITM core powers the ML670100- and ML671000-processor families that target general-purpose, computer-peripheral, and Internet applications. Oki's proprietary nX-8-500S RISC CPU core powers the MSM66573 16-bit CMOS microcontroller, which integrates a 10-bit A/D converter, multifunction timers, PWM, and serial ports. The MSM66573 family targets the system control of small, low-power devices. MSM66573/66573L is a 64-kbyte mask-ROM version, and the 64-kbyte MSM66Q573/66Q573L embedded-flash-memory version is also available.

Power management: The devices have three operating modes to reduce power consumption.

Special instructions: The ML670100 and ML671000 devices use the ARM and ARM Thumb instruction sets. The MSM66573 devices use Oki's proprietary nX-8-500S instruction set.

Integrated peripherals: Devices may include an 8/10-bit A/D converter, a UART, a synchronous-serial interface, a USB 1.1 controller, DMA, and an internal ROM/RAM.

Development tools: ARM development tools support ML670100 and ML671000 applications. Ashling and Oki offer tools for the MSM66573.

Patriot Scientific Corp (PTSC)

PTSC based the 32-bit Ignite I removed-operand-set-computing microprocessor on the Shboom stack-based architecture and is available as a silicon device or synthesizable core. The microprocessor is architecturally similar to a Java virtual machine and can run Java, C, and Forth code. Zero-operand (stack) architectures eliminate operand bits, resulting in shorter instructions, typically one-fourth the size, and smaller programs. Stacks also minimize register saves and loads within and across procedures, resulting in shorter instruction sequences. The processor can address as much as 4 Gbytes of physical memory and supports virtual memory with external mapping logic.

Special instructions: The Ignite has 12 virtual-processing-unit instructions supporting deterministic operations.

Integrated peripherals: The Ignite includes an eight-channel DMA controller, an eight-level interrupt controller, and a virtual-processing unit.

Development tools: Sun Microsystems' PersonalJava, Wind Rivers' VxWorks, and PTSC's vxPresso software suite of tools are available for development support. The development kit with the Open Service gateways Initiative Suite allows the Ignite to act as a PCI card or as the foundation for a new device.

Philips Semiconductors

THE PHILIPS SEMICONDUCTORS XA (eXtended Architecture) family of 16-bit single-chip microcontrollers provides an upward compatibility path for 80C51 users who need higher performance and 64 kbytes or more of program memory. You can translate 80C51 code to run on XA microcontrollers. The performance of the XA architecture supports the bit-oriented operations of the 80C51 and for multitasking operating systems and high-level languages, such as C.

A high-performance static 80C51 design fabricated with Philips high-density CMOS technology, the 8xC51 contains a 128×8-bit RAM; 32 I/O lines; three 16-bit counters/timers, a six-source, four-priority-level, nested-interrupt structure; a serial-I/O port for multiprocessor communications, I/O expansion, or full-duplex UART; and on-chip oscillator and clock circuits. The device is a low-power, static design, which offers a range of operating frequencies as low as 0 Hz. Because the design is static, you can stop the clock without losing user data. Execution then resumes from the point that the clock stopped.

Power management: Software-selectable idle and power-down modes are available. Idle mode freezes the CPU, allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

Integrated peripherals: Devices can include DRAM controller, brownout detection, analog comparators, power-on reset, capture/compare, and controller-area network.

Development tools: Philips Semiconductors' Microcontroller Toolbox contains development tools for each microcontroller. Some of these tools are available from Philips, but most are available from third-party companies.

picoTurbo

The fully synthesizable, 32-bit pT-100Ax and pT-110Ax RISC processors target MP3-player, personal-digital-assistant, cellular-phone, smart-card and system-on-chip applications. They are available as RTL source code in Verilog HDL along with synthesis scripts, synthesized gate-level netlists, and GDSII netlists to support soft, firm, and hard formats. The cores are compatible with the ARM v4T instruction set and support the Advanced High-performance Bus protocol described in the AMBA (Advanced Microprocessor Bus Architecture) bus specification, Revision 2.0. The five-stage pipeline supports an instruction per cycle operation. The pT100Ax core includes a single-cycle multiple-accumulate unit. The pT-110Ax core provides a fully programmable cache ranging from 1 to 64 kbytes in 2-kbyte increments. In addition to the primary caches, the pT-110Ax also contains separate instruction and data scratchpad caches that are programmable at 256 bytes and 2 kbytes.

Power management: If the pipeline is empty for more than five clock cycles, the power-management logic automatically places the processor in a low-power state. When no multiply/multiply-accumulate instruction is in the five-cycle pipeline, clock gating disables the multiplier unit to save power.

Special instructions: These cores are compatible with the ARM v4T instructions and support 16-bit Thumb mode for code compression.

Integrated peripherals: The optional picoPack platform IP (intellectual property) is a collection of AMBA-based, reusable, peripheral-IP blocks and includes AHB2PCI, AHB3APB, and AHB2VCI bridges; flash-memory, SRAM, SDRAM, and internal-memory interfaces; timers and watchdog timers; an arbiter; an LCD controller; an HDLC controller; and an interrupt controller.

Development tools: Third-party tools, such as ThreadX, Majic, Design Compiler, and Verilog-XL, support these cores.

PMC-Sierra MIPS Processor Division

THE 64-BIT RM5200, RM7000, AND RM9000X2 FAMILIES MIPS RISC microprocessors are compatible with the MIPS-64 instruction-set architecture. RM5200A devices can simultaneously execute one integer and one floating-point instruction in a single clock cycle. The chips include 32 kbytes each for independent instruction and data caches and provide external-peripheral and -memory access at bus

speeds exceeding 100 MHz. RM7000 devices feature a L2 cache for LAN and WAN applications and can simultaneously execute two integer instructions or one integer with one floating-point instruction. These processors integrate 256 kbytes of L2 cache, as well as 16 kbytes each for independent L1 instruction and data caches. The RM7000A contains an L3 cache controller for accessing as much as 8 Mbytes of external cache.

The RM9000x2 integrated multiprocessor includes enhancements for networking, offering tightly coupled L1/L2 caches with deterministic access times, a seven-stage pipeline that allows a 1-GHz pipeline frequency, and sophisticated branch prediction. The five-state MOESI (modified shared/exclusive/shared/invalid protocol maintains cache coherency, and all cache transfers between CPUs occur at the CPU's pipeline frequency. HyperTransport and SysAD interfaces support hardware-I/O coherency, enabling I/O devices access to coherent memory. The 160-Gbps shared-memory, multipoint switch fabric connects the CPU sub-system with the memory and I/O interfaces and allows simultaneous accesses to all ports. The 200-MHz DDR-SDRAM interface provides 25.6 Gbps of memory bandwidth, and the HyperTransport and SysAD interfaces provide easy connection with a range of high-speed networking peripherals. A local bus provides connectivity to lower speed devices. The vectored, prioritized interrupt controller supports 256 mappable, external, and interprocessor interrupts to support multiprocessing. The on-chip EJTAG debugging module supports hardware and software debugging.

Special instructions: The floating-point unit supports three-operand multiply, double-precision multiply, and double-precision multiply-accumulate instructions.

Integrated peripherals: The Galileo System controller supports a variety of integrated peripherals. Devices include integrated DDR SDRAM, HyperTransport, SysAD, and local-bus interfaces.

Development tools: Some devices support EJTAG debugging with trace buffers on each CPU core. Wind River and Corelis offer development tools.