

Rabbit Semiconductor

The 8-bit Rabbit 2000 microprocessor operates as fast as 30 MHz and has numerous on-chip peripherals, including four serial ports and a battery-backed real-time clock. Other features include glueless interfacing to memory and I/O devices, remote cold boot-up, three levels of interrupt priority, 40 parallel I/O lines, five 8-bit timers, and one 10-bit timer with two match registers.

Power management: The Rabbit 2000 has a low-power, “sleepy” mode of operation. Once in the sleepy mode, the Rabbit continues to slowly execute instructions with a reduced current consumption. It also has six programmable-processor-clock modes and programmable wait states. A separate power pin for the real-time clock can shut down the processor while keeping the clock alive.

Special instructions: The Rabbit 2000 features an enhanced 64180/Z180-style architecture, eliminating the obsolete or little-used 64180/Z180 instructions and adding 1-byte operation codes for 16-bit logical and arithmetic operations, including compact instructions for 16-bit indexed loads and stores.

Integrated peripherals: Four flexible serial ports eliminate the need to add interface chips. An on-board slave port allows the Rabbit to act as an intelligent peripheral device. The Rabbit has a full array of configurable timing devices, including five 8-bit timers, one 10-bit timer, a real-time clock, a watchdog timer, and a periodic-clock interrupt.

Development tools: Z-World's Dynamic C, an interactive compiler, editor, and source-level debugger, supports software development for the Rabbit 2000. Dynamic C and the Rabbit 2000 can handle applications exceeding 50,000 C statements. The Rabbit 2000 instruction set accommodates Dynamic C's optimization requirements, reducing the need for assembly-language programming.

SandCraft

The two-way-superscalar SR70000 family MIPS64 microprocessors have a nine-stage pipeline and target networking, image-processing, and Internet-server applications. The processor can operate as fast as 800 MHz, and includes dual-instruction fetch, instructions having as many as six issues and as many as six executes, and dual commit to sustain an instruction-throughput rate of two instructions per cycle. Integrated on-chip 512kbyte L2 cache, L3 cache controller, and L3 cache tags maximize system performance. The system interface is compatible with the R4xxx, 5xxx, and 7xxx SysAD interfaces and can operate as fast as 133 MHz with split transactions and out-of-order return. The floating-point unit is MIPS64-compliant.

Power management: A fully static design supports dynamic power saving features to minimize power consumption.

Special instructions: The devices have instructions for integer multiply-accumulate, integer rotate, and clamping.

Development tools: Compilers for software development are available from Red Hat and Cygnus. The Linux and VxWorks operating systems are available. SandCraft and Marvell offer development boards.

Sharp Microelectronics of the Americas

The 32-bit, ARM922T-based LH7A400 system on chip targets applications for color-multimedia and portable systems. The 32-bit, ARM720T-based LH79520 system on chip targets applications for color LCDs. The 32-bit, ARM7TDMI-based LH754xx microcontroller system-on-chip family targets applications for black-and-white or gray-scale LCDs. The 8051-based, 8-bit LZ87010 microcontroller system on chip offers equivalent performance to a 288-MHz standard 8051. These devices operate over the industrial-temperature range of -40 to $+85^{\circ}\text{C}$.

Power Management: Depending on the device, three or five modes support reduced power consumption and range from scaling the clock frequency, combinations of CPU and peripherals active or disabled, to disabling all clocks including the real-time clock.

Special instructions: The LZ87010 has an extended move instruction that enables software to write to code-memory space.

Integrated peripherals: Devices support a combination of functional blocks and can include an MMU, a DMA controller, a vectored interrupt controller, serial and parallel interfaces, counters/timers, a real-time clock, a watchdog timer, PWM, infrared support, an on-chip PLL, SRAM/flash/ROM controller, PCMCIA, UARTs, SPI, a 12-bit A/D converter, an 8-bit D/A converter, a touchscreen controller, a watchdog timer, a low-voltage detector, and JTAG support. Some family devices include CAN2.0b or the ability to also control color supertwist-nematic, double-metal-twisted-nematic, thin-film-transistor, and high-resolution-thin-film-transistor LCDs.

Development tools: In-circuit emulators and full evaluation boards with I/O cards and LCD panels support hardware development. Green Hills and any ARM development suite offer software-development tools. Most devices support debugging features, such as hardware breakpoints, trace, and view and modify registers and memory. A low-cost debugging tool takes advantage of these on-chip debugging features through a two-wire debugging interface.

Silicon Storage Technology

SST's FLASHFLEX51 PRODUCTS provide alternatives to one-time-programmable or nonprogrammable ROM-based microcontroller products. The SST89C54 and SST89C58 microcontrollers, respectively, embed 20 and 36 kbytes of SuperFlash EEPROM in two internal-flash-memory blocks. This dual-memory-block architecture permits in-application programming that allows the CPU to run user programs from one block while serving a flash-programming operation in the background on the other block. These products also support extended security modes with SoftLock for software-piracy prevention and inadvertent write protection.

Power management: FlashFlex51 devices support a power-down mode with wake-up on external interrupt.

Integrated peripherals: FlashFlex51 devices are pin-for-pin compatible with standard 8xC5x microcontrollers.

Development tools: SST's Boot-Strap Loader and EasyIAP example program allow users to install their application code into a product. Third-party 8051-development tools support software development.

STMicroelectronics

STMICROELECTRONICS OFFERS a range of processor families. The ST6 family targets low-range to mid-range, 8-bit embedded-control applications that need high noise immunity. Registers and peripherals are memory-mapped in the chip's address space requiring only program read or writes to configure or communicate with a peripheral. The ST7 family is an 8-bit microcontroller that targets smart appliances, motor control, automotive body, and home automation. The X and Y index registers support indexed addressing modes and simplify branching routines and data modifications. The ST7261/2/3B flash devices comprise a ST7 core integrated with low-speed USB. The ST7265 supports full-speed USB with an emphasis on flash-media-card mass-storage applications and supports the Bulk-Only-Transfer and the Control, Bulk, Interrupt protocols. The ST9 family targets the gap between high-end, 8-bit and low-end, 16-bit applications. The MMU lets you linearly address as much as 4 Mbytes of program and data memory. The 256-byte register file, organized as 14 sets of 16 8-bit registers, supports switching from one set of registers to another to permit fast context switching. Although the ST9 has an 8-bit ALU, the chip handles 16-bit operations, including arithmetic, loads/stores, and memory-to-register and memory-to-memory exchanges. The ST10 processor core, a 16-bit-instruction-word CMOS microcontroller, targets custom system-on-chip products, such as hard disks, CD-ROM drives, DVD, car-radio devices, and engine-management units. The ST10F269 integrates a multiply-accumulate unit with automotive-specific peripheral blocks, such as CAN interfaces and two watchdog timers—one to monitor the clock oscillator and one to monitor the program execution.

Power management: Each device family supports various power-reduction modes and include stopping peripherals; clocking the processor and peripherals at a lower frequency; stopping the core while leaving the peripherals at full or reduced speed; or stopping the oscillator, core, and peripherals. These modes maintain RAM and enable an interrupt to wake the processor, and some devices can use a real-time clock to wake the processor after a certain period.

Special instructions: The accumulator-based ST6 has increment and decrement instructions that can access both memory and registers without passing through the accumulator. The ST7 supports true bit manipulation and has an 8×8-bit, unsigned multiply instruction. The ST9 includes support for BCD and Boolean formats and has instructions to facilitate large-program and -data handling through the MMU and to improve code density of C function calls. The ST10 supports single-cycle instructions for 16- and 32-bit signed arithmetic.

Integrated peripherals: The STx device families offer various combinations of the major functions necessary for embedded control, including an RC oscillator; a 32-khz internal oscillator; safe power-on; a safety oscillator; 8/10-bit A/D converters; data EEPROM; flash, LED, and LCD drivers; SPI; a UART; autoreload timers; PWM; and multifunctional bidirectional I/O lines. Additional peripherals on the ST9 and ST10 series can include CAN 2.0B and J1850 interfaces, programmable asynchronous and synchronous capability, an associated address/wake-up option, and DMA channels.

Development tools: STMicroelectronics offers development tools; including starter kits; in-circuit emulators; programming boards; an assembler; a linker; a C compiler; and function libraries, including USB, a debugger, and simulators. Cosmic, Keil, Metrowerks, Raisonance and Tasking, provide third part support for software development. Hitex, Lauterbach and Nohau provide third-party support for hardware development. The ST6-Realizer automatic code generator allows developers to generate code without knowledge of the ST6.

Sun Microsystems

THE ULTRASPARC IIE MEMBER of Sun Microsystem's UltraSPARC II RISC processor family implements the full SPARC Version 9 architecture plus the VIS instruction set to accelerate small integer operations and provide special-purpose instructions. The CPU uses 64-bit address arithmetic and contains an MMU that translates 44-bit virtual addresses to 41-bit physical-memory addresses with 64-bit address pointers. The devices have 64-byte block load and store instructions that use the 64-bit datapaths and registers inside the processor, supporting high-performance memory-to-memory bandwidth. The processor includes an SDRAM controller that supports PC-100-type SDRAM DIMMs and a 32-bit, 66-MHz PCI-bus interface, which is compatible with the PCI specification Version 2.1.

Power management: The UltraSPARC Iie complies with the Energy Star initiative, supports wake-on-PCI activity, and implements a sleep mode that shuts down external devices and self-refreshes the SDRAM. PLL support and one-sixth modes as well as a stick register (PCI clock/10) for constant clock reference are also available.

Special instructions: The VIS RISC instruction set extends the SPARC Version 9 architecture and accelerates multimedia, image-processing, and networking applications. Sun's medialib, a multimedia performance library, supports the VIS instructions via assembler, C functions, or macros.

Integrated peripherals: The UltraSPARC Iie has an integrated 256-kbyte L2 cache.

Development tools: Forte Developer products deliver an integrated environment that provides a full set of graphical tools to create and maintain C, C++, and Fortran applications.

Tensilica

THE 32-BIT XTENSA RISC synthesizable processor architecture targets high-volume, embedded applications. Designers use the Xtensa Processor Generator to configure and extend a family of core processors with special functions for their designs, while performing software development and testing. The Xtensa Processor Generator supports a choice of Gnu-based or Xtensa software-tool suites to match each configured processor. With each new processor configuration, the architecture automatically creates the software-development environment, the instruction-set simulator, bus-functional model, RTOS OSKit, Vectra-DSP libraries, EDA-tool scripts, and the Xtensa Multiprocessor System Modeling API. Xtensa's TIE (Tensilica Instruction Extension) compiler supports designer-defined instruction creation. Optional blocks include a configurable Vectra-DSP unit, a floating-point unit, and multiplier blocks. EEMBC (EDN Embedded Microprocessor Benchmark Consortium) benchmarks with 200-MHz configurations are 193.6 for ConsumerMark, 8.5 for NetMark, and 85.7 for TeleMark.

Power management: Using functional clock gating and a special wait instruction, the processor sets the interrupt-level and power-down clocks to most of the core. The processor awakes at the occur-

rence of the interrupt.

Special instructions: Special instructions for the Vectra DSP or the multiply-accumulate-16 option are available in addition to the 80 16/24-bit basic RISC instructions. The TIE compiler implements new instruction-set extensions for optimizing application performance. The resulting HDL is correct-by-construction and has compiler, assembler, simulator, and debugger support.

Integrated peripherals: Basic peripherals include timers and interrupt controller.

Development tools: The same database generates both the Xtensa software-development environment and the hardware description to ensure correctness and consistency at construction. The TIE compiler translates designer-defined TIE-language descriptions into additional software-tool and hardware components. The tools also include a bus-functional model for cosimulation, the OSKit for RTOS work, instruction-set simulator for single-processor or multiprocessor system modeling, and an emulation kit.

Texas Instruments

THE MSP430X SERIES OF DEVICES are 16-bit RISC microcontrollers. MSP430x1xx derivatives include a range of in-system-programmable devices with 1 to 60 kbytes of flash, a 12-bit ADC, a multiplier, USARTs, and 10 PWM channels. MSP430x3xx derivatives include a range of devices that include a segment-type LCD driver and offer OTP for low-volume and factory-masked ROM. These devices target high-volume OEMs that ultimately require cost-effective ROM. MSP430x4xx derivatives include a range of in-system-programmable flash devices that integrate a segment-type LCD driver and can operate in a standby mode with a real-time-clock function active at less than 1 μ A. The MSP430x4xx family targets portable-battery-powered-measurement applications that require an LCD.

Power management: The asynchronous clock system supports two external crystals and a third independent on-chip digitally controlled oscillator that supports start-up and synchronization in less than 6 μ sec. This approach allows an MSP430 to extensively remain in low-power standby modes and quickly respond to interrupt-driven events. In many applications, a single 32-kHz watch crystal with the on-chip digitally controlled oscillator is sufficient for low-rate operation.

Special instructions: All MSP430 derivatives use the same 27 RISC instructions and seven orthogonal addressing modes. The devices require no special instructions to support the entire memory map.

Integrated peripherals: Available peripherals include a 16-bit watchdog timer, a 16-bit PWM, asynchronous serial-communication support, a 16-bit timer, shadow registers, a USART, a multiplier, a 12/14/16-bit A/D converter, a voltage-reference and temperature sensor, and a separate analog comparator.

Development tools: TI's flash-emulation tool supports development and uses an integrated development environment to access the device's on-chip JTAG port for in-circuit emulation. The tools support peripheral access, programming, single-stepping, breakpoints, and full-speed operation. IAR provides a C compiler, and Hitex provides an in-circuit emulator. Evaluation kits are available for all MSP430x3xx devices.

Toshiba America Electronic Components

TOSHIBA BASED THE TX49, TX39, AND TX19 FAMILIES of processors on the MIPS 64-and 32-bit RISC architectures. The TX49 series targets office-automation and network-equipment applications and have EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium) scores available. The TX39 targets personal-digital-assistant applications, and the TX19 series targets applications requiring real-time control. These devices implement the MIPS I, II, and III instruction-set architecture, and some integrate a floating-point unit. The 16-bit TLCS-900/H series microcontrollers target real-time-control applications and offer a 16-bit ALU, a 4-byte instruction-queue buffer and four banks of 32-bit general-purpose registers. The 8-bit TLCS-870/C series microcontroller family targets portable-consumer-electronic equipment that requires low-voltage, low-power, and low-noise features.

Power management: Low-power modes range from dynamically stopped or slowed clock rates for the CPU and, optionally, the peripherals.

Integrated peripherals: Some devices include flash and SDRAM controllers, ROM, 32-bit PCI,

PCMCIA, DMA, serial I/O, parallel I/O, PWM, timers/counters, a real-time clock, a watchdog timer, an AC'97 Interface, a CAN, UARTs, I²C, 8/10-bit A/D converters, LED drivers, and color/monochrome LCD controllers.

Development tools: Toshiba offers a starter kit; a build manager that includes a C compiler, assembler, and linker; a full in-circuit emulator; and CaseWorks, which includes source-analysis, memory-allocation, module-structure and flow-chart tools. Third-party development tools are available from Red Hat, Green Hills, Cygnus Solution, Agilent, and Wind River.

Transmeta Corp

THE X86-COMPATIBLE CRUSOE TM5800 AND TM5500 microprocessors target handheld- and mobile-computing applications. Low-power operation relies on Code Morphing, a software process that dynamically translates x86 instructions into VLIW (very-long-instruction-word) instructions for the underlying Crusoe hardware engine. The Code Morphing software resides in flash ROM and is the first application to launch when you power up the Crusoe processor. Upon completion of Code Morphing's initialization, other system software components, such as the BIOS and operating system, load in traditional fashion.

Power management: Transmeta's LongRun power-management technology allows Code Morphing software to adjust Crusoe's voltage and clock frequency on the fly, depending on the demands that software places on the Crusoe processor, resulting in reduced power consumption. The Code Morphing software implements the LongRun policies that continuously scale both the frequency and the voltage of the Crusoe processor according to the instantaneous demands of the computer system. It can detect scenarios based on runtime performance information and then, transparently to the user, adapt its power usage accordingly.

Special instructions: The Crusoe is x86-instruction-compatible.

Integrated peripherals: Crusoe microprocessors provide single- and double-data-rate DRAM controllers that can operate simultaneously or individually.

Triscend

THE TRISCEND E5 CONFIGURABLE-SOC FAMILY comprises five accelerated, 8051-based microcontrollers that vary in the amount of on-chip programmable logic, RAM, and I/Os. The A7 configurable-SOC family is similar to the E5, except that the A7 family uses the 32-bit ARM7TDMI processor core. These devices target embedded applications that demand high levels of customization and are compatible with third-party tools that support their respective core architectures—from code development to in-system, real-time debugging. Designers customize the SOC peripherals with the Triscend FastChip development system using a drag-and-drop method, enabling the creation of 8051 or ARM7 derivatives on demand. Designers select the desired soft peripheral and then "drag" it into place around the processor. FastChip automates the rest of the process so that code development can proceed without your worrying about the implementation details of the soft peripheral.

Power Management: The devices support programmable power-management modes to control power consumption.

Special instructions: The A7 supports 16-bit instructions in the Thumb state for higher code density.

Integrated peripherals: These devices contain on-chip programmable logic, a two-channel DMA controller, 256-byte scratchpad RAM, a JTAG interface, and a hardware breakpoint unit. The A7 also includes 16-bit timers, 16C550-style UARTs with a modem interface, interrupt control, a 32-bit watchdog timer, and external flash and SDRAM interfaces.

Development tools: These devices are compatible with third-party tools that support their respective core architectures. Both families have on-chip JTAG interface and hardware breakpoint unit for dedicated in-system debugging. The E5 supports integration with Keil Software's uVision2. The A7 includes advanced debugging support via Wind River the VisionProbe II and the VisionClick source-level debuggers that provide visibility into the ARM7TDMI core and into the on-chip programmable logic. The SRAM can double as a trace buffer during debugging. Triscend offers hardware/software-development boards and low-level drivers and board-support packages for eCos and VxWorks.

Ubicom

THE HEART OF THE IP2022 is a 100-MIPS RISC engine that integrates on-chip high-speed flash memory and SRAM. Two full-duplex serializer/deserializers decode data over a variety of high-speed communication interfaces to support LAN bridging and gateway applications. Implementing traditional hardware functions in software, the device supports in-system programming and reprogramming using prebuilt software modules and configuration tools, including device programming over the network. Ubicom provides a software-development kit that includes a variety of prebuilt ipModule-software functions, including Ethernet-media-access-controller/physical-layer and TCP/IP stack modules, USB, and multichannel UARTs. These software ipModules are typically communications-centric and use on-chip, hardware-assisted peripheral blocks or general-purpose-I/O pins to implement additional peripheral features.

Power management: The IP2022 includes a sleep capability with a watchdog timer and a multi-input wake-up, supports 32-kHz oscillator operation, and can change the clock speed on the fly via a speed instruction.

Special instructions: A speed instruction changes the processor execution speed on the fly by dividing down the core clock by factor of one to 128.

Integrated peripherals: Peripheral support includes two full-duplex serializer/deserializers; two full-duplex linear-feedback-shift registers for CRC and data whitening; an 8/16-bit parallel-port interface; an external RAM-expansion bus; an eight-channel, 10-bit A/D converter; and ISP (Internet-service-provider) and ISD (in-system-debugger) support.

Development tools: The IP2022 contains on-chip ISD and ISP support. Ubicom offers the Unity integrated development environment that includes the GnuPro tool chain from Red Hat, a software-development kit with an application-configuration tool, OS support, a development board, and an ISP/ISD dongle.

Xemics

The low-power, low-voltage, 8-bit XE8000 series of CMOS microcontrollers have some analog features. These devices use the CoolRISC processor core that has a separate 22-bit instruction bus and 8-bit data bus. All instructions, including an 8×8-bit multiply, execute in a single cycle. XE8000 devices target portable, battery, and RF-powered applications, including automation and sensor interfacing.

Power management: The RC oscillator can run as low as 32 kHz, decreasing the power consumption as the frequency decreases. The digital components are voltage-regulated to limit power dissipation. Multiple-time-programmable instruction-memory circuits operate from 2.4 to 5.5V, and ROM circuits start at 1.2V.

Special instructions: The processor performs single-cycle instruction execution for multiply, jump, and conditional jump.

Integrated peripherals: Peripherals include a UART, a 12/16-bit A/D converter, a prescaler, counters, an analog-switch matrix, a dual oscillator, and LCD drivers.

Development tools: Complete development tools include programmers/starter kits, an ICE, and C compiler.

Xilinx

XILINX'S 32-BIT MICROBLAZE SOFT-PROCESSOR CORE runs in an FPGA that runs at 125 MHz and targets the networking, telecommunication, data-communication, embedded, and consumer markets. The processor features a RISC architecture with Harvard-style separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory. MicroBlaze uses approximately 800 to 900 logic cells and, with the Virtex and Virtex-II Platform FPGAs, system designers can implement high integration on a single device.

Special instructions: Designers can add or modify the instruction set with custom instructions, including DSP functions, such as FFT and multiply-accumulate. On Virtex-II devices, the multipliers

embedded in the FPGA fabric can execute a two-cycle 32×32 -bit multiply instruction.

Integrated peripherals: The MicroBlaze development kit contains IBM CoreConnect-enabled peripherals, which include timer/counters, a watchdog timer, a UART, an interrupt controller, general-purpose I/O, an arbiter, and external-flash and SRAM interfaces. These peripherals are parameterizable. Other peripherals include a 10/100 Ethernet media-access controller, SPI, I²C, and ATM Utopia level 2.

Development tools: In addition to Xilinx tools to parameterize and build a processor platform, the MicroBlaze kit contains a complete set of Gnu-based software tools, including a compiler, an assembler, and a debugger.

Zilog

THE NEXT GENERATION eZ80 system on chip can serve Web pages over a TCP/IP network, allowing system monitoring and control, remote processor-code updates, and system compatibility. Any browser with network access can control and monitor a network application. The eZ80 executes Z80 code four times faster than traditional Z80s at the same clock speed and can operate at speeds as high as 50 MHz. The eZ80 can linearly address 16 Mbytes without a memory-management unit. The Web server features an embedded Internet-software suite that enables the transmission and reception of HTML form data and the dynamic generation of Web pages.

The 8-bit, OTP Z80 programmable EPROM microcontroller integrates RAM and peripherals, featuring enhanced wake-up circuitry, programmable watchdog timers, low-noise EMI options, external memory, analog comparators, A/D converter, timers, and low current sleep mode in a register-to-register architecture.

Power management: The Z80 supports sleep and halt modes.

Special instructions: The eZ80 includes block-move instructions.

Integrated peripherals: Devices can include UART, SPI, I²C, an A/D converter, and comparators. The eZ80 includes a watchdog timer, DMA, an on-chip crystal oscillator, a Zilog debugging interface, and a 16×16 -bit multiply accumulator.

Development tools: Internal and third-party development tools for the eZ80 include C compilers, evaluation boards, and emulators in an integrated development environment. Third-party partner IAR also offers MakeApp, a program that generates peripheral driver code.