



## 8-BIT MICROPROCESSORS

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Analog Devices</b> www.analog.com Enter No. 341	ADuC812	16	External: 16/8 code, 24/8 data	8	3/5	48 mW (3V)	15 to 150 $\mu$ W			
	ADuC816 ADuC824	12.58	External: 16/8 code, 24/8 data	8	3/5	25 mW (3V)	60 $\mu$ W			
<b>Atmel</b> www.atmel.com Enter No. 342	AVR	1 to 24	16/8	16	1.8 to 5.5	1 to 3 mA	Less than 1 $\mu$ A	8 $\times$ 8-bit unsigned, 16 $\times$ 16-bit signed	Two-cycle 8 $\times$ 8 fixed point	
	MCS 51AT 89 family	12 to 33	8	16	2.7 to 6	80 mW	Idle: 2 mA, power-down: 12 $\mu$ A	8 $\times$ 8-bit		
<b>Cybernetic Micro Systems</b> www.ControlChips.com Enter No. 343	8051	51	20/8	8, 16, 32	3.3/5 tolerant	150 mW		Yes		
<b>Cygnal Integrated Products</b> www.cygnal.com Enter No. 344	C8051F00X C8051F01X C8051F02X	25	16/8	8	2.7 to 3.6	27 to 34 mW	Software control: 1 to 15 $\mu$ A	8 $\times$ 8-bit		
	C8051F2XX	25	16/8	8	2.7 to 3.6	27 mW	Software control: less than 15 $\mu$ A	8 $\times$ 8-bit		
<b>Cypress Microsystems</b> www.cypressmicro.com Enter No. 345	CY8C25122 CY8C26233 CY8C26443 CY8C26643	24	8	8, 16, 24	3.3/5	20 mA	Analog, digital, both	Multiply-accumulate unit		
<b>Fujitsu Microelectronics</b> www.fmi.fujitsu.com Enter No. 346	F2MC - 8L	1 to 12.5	16/8	8	1.8 to 6	50 mW	Sleep, stop, subclock, watch	Two 16-bit accumulators		
<b>Intel Corp</b> www.intel.com Enter No. 347	MCS-251	16, 24	24/8	16 internal, 8 external	4.5 to 5.5	85 mA	Idle, power-down	16 $\times$ 8-bit		
	MCS-51	12, 16, 24, 33	8	8	4.5 to 5.5 $\pm$ 10%	24 mA	Idle, power-down	8 $\times$ 8-bit		
<b>Microchip Technology Inc</b> www.microchip.com Enter No. 348	Eight-pin, 8-bit family	10	14/8	12	2.5 to 5.5	10 mW	Standby	8 $\times$ 8-bit		
	PIC16CX	20	14/8	14	2 to 6	50 mW	Standby			
	PIC18XXX	40	16/8	16	2.5 to 5.5	50 mW	Standby	8 $\times$ 8-bit		
<b>Mitsubishi Electric &amp; Electronics USA</b> www.mitsubishichips.com/startMCU.html Enter No. 349	740	32 kHz to 20 MHz	16/8	8	1.8 to 5.5	40 mW	Standby: 35 $\mu$ W, sleep: 0.5 $\mu$ W	Software multiply		
<b>Motorola Inc</b> www.motorola.com/semiconductors Enter No. 350	68HC05 family	2.1 to 4.0	8	8	2.2 to 5	25 mW (2 MHz)	Wait, stop			
	68HC08 family	2.1 to 4	8	8	2.2 to 5	75 mW (8 MHz)	Wait, stop			
	68HC11 family	Up to 5	8	8	3, 5	124 mW (3 MHz)	Wait, stop			

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
8-kbyte code flash/EE, 640-byte data flash/EE, 512-byte SRAM			52 PQFP	Three 16-bit	UART, I <sup>2</sup> C, SPI, four 8-bit digital I/O ports	Nine	Eight-channel, 12-bit	ADC data DMA to external data memory	\$6.85
8-kbyte code flash/EE, 640-byte data flash/EE, 512-byte SRAM			52 PQFP	Three 16-bit	UART, I <sup>2</sup> C, SPI, 26 parallel I/O	12	Two	On-chip transducer-burn-out current sources	\$8.01 to \$9.33
1- to 128-kbyte flash, 64-byte to 4-kbyte EEPROM, 128-byte to 4-kbyte SRAM			8/20/28/40 DIP, 32/44/64 TQFP, 20 SSOP, 8/20 SOIC	Two 8-bit, two 16-bit	SPI, UART, I <sup>2</sup> C, 8-bit parallel (64-kbyte addressing)	27 internal, eight external	Eight-channel, 10-bit	JTAG debug	50 cents to \$4
1- to 32-kbyte flash, 2-kbyte EEPROM, 128- to 512-byte SRAM			20/40 PDIP, 20 SOIC, 44 TQFP	One to three 16-bit	SPI full-duplex UART			In-system-programmable flash, three-level lock-bit security	\$1 to \$3
4-kbyte dual-port RAM, 8-kbyte program RAM			100 SQFP	Three 16-bit	One, four 8-bit parallel ports	Seven		Breakpoint/single-step debug, software-select EISA interrupt-request host interrupt	\$12
32- or 64-kbyte ISP flash for program/data, 256-byte SRAM, 2- or 4-kbyte XRAM			32 LQFP, 48/64/100 TQFP	Four or five 16-bit, programmable counter array with five capture modules, watchdog	SPI, SMBus, one or two UARTs, as many as 64 parallel I/Os	21 (two levels)	Eight-channel, 12-bit, two 12-bit DACs		\$8 to \$13
8-kbyte ISP flash for program/data, 256-byte SRAM, 1-kbyte XRAM			48 TQFP, 32 LQFP	Three 16-bit, watchdog	SPI, UART, as many as 32 parallel I/Os	21 (two levels)	As many as 32 channels, 8/12-bit, any/all parallel I/O as source	Two analog comparators	\$3 to \$7
8- or 16-kbyte program flash, 128-byte SRAM			8 PDIP, 20/28/48 PDIP/SSOP/SOIC, 48 QFP	As many as eight user-definable 8/16/24/32-bit, PWM	As many as four user-definable SPI/synchronous, six to 44 parallel I/Os	16	One or two eight-channel ADC/DACs	User-definable filters, amplifier/scalers, comparators	\$1.58
4- to 60-kbyte, 128-byte to 18-kbyte SRAM			28-100 QFP/QFP/SOP/SDIP/DIP (plastic)	8/16-bit, 21-bit timebase, 8-bit PWM, PPG, PWC, watchdog	Two serial I/O, I <sup>2</sup> C, USB, two UART, 85 parallel I/Os	10 internal, as many as 16 external	Eight channels, 10-bit	Buzzer output, remote-control carrier generator, DTMF generator, LCD driver	\$1.35 to \$4.50
8- or 16-kbyte OTP, ROM, 512- or 1024-byte RAM			44 PLCC, 40 PDIP	Three 16-bit, watchdog	One or two UARTs	Eight (four levels)		Programmable counter array, 40-byte register file	\$3.63 to \$4.57
8-, 16-, or 32-kbyte EPROM, OTP, ROM, 256- or 512-byte RAM			44 PLCC/PDIP/MQFP	Three 16-bit, watchdog	Full-duplex UART/serial I/Os	Eight (two levels)		Programmable counter array	\$1.30 to \$3.25
768- to 3584-byte OTP, 256-byte flash, 16-byte EEPROM, 25- to 128-byte SRAM, up to 128-Mbyte EDO DRAM			8 PDIP/SOIC/CERDIP	8-bit real-time clock/counter (8-bit programmable prescaler)	UART, I <sup>2</sup> C and other interfaces buffers; microcoded		As many as four channels, 8/10-bit	In-circuit serial programming, low-voltage detect, brownout reset	80 cents to \$2
896-byte to 14-kbyte OTP, 36- to 368-byte RAM			18 to 44 DIP/SOIC/SSOP/PLCC/TQFP/MQFP	10-bit PWMs, 8/16-bit watchdog	USART, I <sup>2</sup> C, SPI, master and slave I <sup>2</sup> C, 13 to 33 parallel I/Os	Four to 12	Four to eight channels, 8/10-bit	In-circuit serial programming, low-voltage detection, brownout reset	\$1.35 to \$5.50
16- to 32-kbyte OTP, 512- to 1536-byte SRAM			8 to 84 DIP/SOIC/PLCC/TQFP	Two 10-bit PWM, three 8/16-bit watchdog, start-up, power-up	One or two UARTs, three-wire SPI, I <sup>2</sup> C, master and slave I <sup>2</sup> C, 23 to 68 parallel I/Os	As many as four external, two UARTs on address bit	10-bit, support during sleep	In-circuit serial programming, low-voltage detection, brownout reset	\$1.60 to \$6.50
4- to 60-kbyte flash, OTP, EPROM, mask, 192-byte to 2-kbyte SRAM			32 to 144 PQFP, 32 to 64 SDIP	One to four 8-bit, zero to two 16-bit, zero to two PWMs, watchdog	UART, one or two serial I/O, I <sup>2</sup> C, CAN, USB, 29 to 72 parallel I/Os	As many as nine external	As many as 13 channels, 10-bit, DAC	LCD, key-on wake-up	\$1 to \$10
1.2- to 32-kbyte OTP, 64 to 920-byte SRAM			SDIP, SOIC, CLCC/PLCC, DIP, CDIP, QFP, LQFP	Two 16-bit, multifunction timer, real-time interrupt, event, 8-bit IR, timebase	SCI, I <sup>2</sup> C, Mbus, timebase SPI, USB, serial I/Os, CAN, as many as 80 parallel I/Os	Two plus one/peripheral	8-bit		70 cents to \$18
1- to 64-kbyte flash, 64 to 920-byte SRAM			SDIP, SOIC, CLCC, PLCC, DIP, CDIP, QFP, LQFP	Two 16-bit, multifunction timer, real-time interrupt, event, 8-bit IR, timebase, PWM	SCI, I <sup>2</sup> C, Mbus, SPI, USB, serial I/Os, CAN, as many as 51 parallel I/Os	Two plus one/peripheral	8- or 10-bit	Monitor mode, temperature sensor, comparator, high-current drive	\$1 to \$10
4- to 32-kbyte OTP, 192-byte to 1-kbyte SRAM			DIP, CDIP/PDIP, CLCC/PLCC, QFP, LQFP	As many as four 16-bit, real-time interrupt, pulse accumulator	SCI, SPI, 38 parallel I/Os	18	8-bit		\$2 to \$15

## 8-BIT MICROPROCESSORS (CONTINUED)

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Philips Semiconductors</b> www.philips.semiconductors.com Enter No. 351	80C51 family	12 to 33	16/8	8	2.7 to 5.5					
<b>Rabbit Semiconductor</b> www.rabbitsemi.com Enter No. 352	Rabbit 2000	30	20/8	8, 16	2.5 to 5	96 mA (5V)	Sleepy	16×16-bit		
<b>Sharp Microelectronics of the Americas</b> www.sharpsma.com Enter No. 353	LZ87010	48	16/8, 8	8 to 24	3.3	40 mW	Idle: 700 μW, power-down: 3.3 μW	8×8-bit		
<b>Silicon Storage Technology Inc</b> www.ssti.com Enter No. 354	FlashFlex51	Up to 33	16/8	8	2.7 to 5	100 mA	Power-down: 40 mA			
<b>STMicroelectronics</b> www.st.com Enter No. 355	ST6	8		8 to 24	3 to 6	3.3 mA	Wait: 350 μA, stop: 0.1 μA			
	ST72254	Up to 8			3.2 to 5.5	5.6 mA	Halt: 10 μA (less than 85°C)/150 μA (less than 125°C)	Yes		
	ST72260, 62, 64	Up to 8			2.4 to 5.5			Yes		
	ST72321J ST72324JK	Up to 8				6.5 mA	Halt: 10 μA (less than 85°C)/50 μA (less than 125°C)	Yes		
	ST72334 ST72314 ST72124	8			3.2 to 5.5	7.4 mA		Yes		
	ST72521				2.7 to 5.5			Yes		
	ST7261 ST7262 ST7263B	1, 2, 4, 8		8 to 32	3 to 5.5	12 mA	Slow, wait, halt	Yes		
	ST7Lite family	Up to 8			2.4 to 5.5	2 mA	Halt, active-halt, wait, slow	Yes		
	ST92F150	24	External: 22/8	8 to 48	4.5 to 5.5	45 mA	Slow: 2.5 mA/MHz, halt/stop: 10 μA	8×8-bit		
<b>Toshiba America Electronic Components</b> www.toshiba.com Enter No. 356	TLCS870/C	32 kHz to 16 MHz	16/8	8 to 40	1.8 to 5.5	5.5 mA	Idle: 2.8 mA, slow: 14 μA, sleep1: 7 μA, sleep0: 6 μA, stop: 0.5 μA			
<b>Triscend</b> www.triscend.com Enter No. 357	E5 configurable family	Up to 40	32/8	8	3.3/5 tolerant		Selective function disable, full power-down: less than 50 μA	8×8-bit		
<b>Uicom Inc</b> www.uicom.com Enter No. 358	IP2022	100	8, external: 8 or 16	16	2.5/2.5 or 3.3, 5 tolerant	130 mA	Yes	One-cycle 8×8-bit signed/unsigned instructions		
<b>Xemics SA</b> www.xemics.com Enter No. 359	XE8000 XE88LC03, 04, 06, 08	4	16/8	22	1.2 to 5.5	1.2 mW	sleep, hibernate	Yes	Three-instruction pipeline	
	XE88LC01 XE88LC02 XE88LC05	Up to 4	16/8	22	2.4 to 5.5	1.2 mW	sleep, hibernate	Yes	Three-instruction pipeline	
<b>Zilog Inc</b> www.zilog.com Enter No. 360	eZ80	50	24/8	24	3.3/5 tolerant	50 mA		16×16+40-bit multiply-accumulate instructions		
	Z8	16	16/8		3 to 5.5	20 mA	Stop: 10 μA	16×16-bit multiply, 32×16-bit divide		

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/ DAC	Additional features	Price (10,000)
2- to 96-kbyte program, 128- to 2948-byte RAM			20 DIP/TSSOP, 44 PLCC/LQFP	Two to four 16-bit	UART, I <sup>2</sup> C				\$1 to \$9
External flash and ROMs, external SRAM	Three chip selects, two out/write enables, up to 6 devices	64180/Z180-style	100 PQFP	Five 8-bit, 10-bit with two match registers, real-time, watchdog	Four asynchronous, two with SPI and synchronous capability, 40 parallel I/Os	Two external		Slave port, bootstrap mode	\$9
64-kbyte flash, 4- plus 256-byte SRAM	SRAM, ROM, flash		100 LQFP	Six 16-bit for capture/compare and PWM, watchdog	Two full-duplex UARTS, I <sup>2</sup> C, 80 parallel I/Os	21	Eight 12-bit	Two 8-bit DAC, 5- $\mu$ sec conversion rate	\$8
20- to 36-kbyte flash, 256-byte to 1-kbyte RAM			40 PDIP, 44 PLCC, 44 TQFP	Three 16-bit, watchdog	UART, four parallel I/Os	Two external			\$2.20 to \$2.42
1- to 8-kbyte OTP, ROM, up to 128-byte EEPROM, up to 320-byte of SRAM			DIP, SDIP, SO, SSOP, QFP	8-bit, 16-bit, 8-bit autoreload, watchdog	UART, SPI	Six-level fixed stack for calls or interrupts	As many as 21 channels, 8-bit	Low-voltage detector	\$1.20
4- or 8-kbyte ROM or flash, 256-byte RAM			28 SO, 32 SDIP	Two 16-bit, PWM, watchdog	SPI, I <sup>2</sup> C	Seven internal, 22 external	Six channels, 8-bit		\$1.93 to \$2.31
4- or 8-kbyte ROM or flash, 256-byte RAM			28 SO, 32 SDIP	Two 16-bit, PWM, watchdog	SPI, I <sup>2</sup> C, SCI	10 internal, 22 external	Six channels, 10-bit		\$1.52 to \$1.87
8- to 60-kbyte ROM or high-density flash, 384-byte to 2-kbyte RAM			32/44 TQFP, 32/42 SDIP	Two 16-bit, PWM, 8-bit autoreload, watchdog	SPI, I <sup>2</sup> C, SCI	10 internal, nine/six external	12 channels, 10-bit		\$2.28 to \$3.49
384- or 512-byte RAM	ROM, flash, EEPROM, ROM		44/64 TQFP44, 42/56 SDIP	Two 16-bit, PWM, watchdog	SPI, SCI	10 internal, 15 external	As many as eight channels, 8-bit	Enhanced reset, external clock	\$2.53 to \$3.22
32- to 60-kbyte flash/ROM, read-out protection, 1- to 2-kbyte RAM			64/80 TQFP	Two 16-bit, PWM, 8-bit autoreload, watchdog	SPI, SCI, I <sup>2</sup> C, CAN	14 internal, 15 external, top-level interrupt	16 channels, 10-bit		\$3.95
4- to 16-kbyte flash, EEPROM, OTP and ROM, 256- to 768-byte SRAM			PDIP, SO, TQFP, CSDIP	16-bit, 8-bit autoreload, 8-bit timebase unit, PWM, watchdog	SCI, SPI, I <sup>2</sup> C, low-speed USB, 11 to 31 parallel I/Os	12 external	Eight channels, 8/10-bit	Low-voltage detector	\$1.51 to \$2.96
1.5- or 8-kbyte (x)flash, 128- or 256-byte EEPROM, 128- to 384-byte SRAM			16/20 SO, 16/20 DIP	One 8-bit, watchdog, real-time, input capture, 12-bit auto-reload, one to four PWMs	SPI	10 internal, four external	Five/seven channels, 8/10-bit	Digital addressable lighting interface communication interface	81 cents to 93 cents
60- to 128-kbyte flash, 2- to 6-kbyte SRAM		Yes	100 PQFP, 64/100 TQFP	Two 16-bit, two extended, watchdog	Two CANs, J1850, two UARTS, I <sup>2</sup> C, SPI	128 vectors, 23 external, seven priorities, nonmaskable interrupt	16 channels, 10-bit		\$4.90 to \$6.50
4- to 60-kbyte ROM, up to 2-kbyte SRAM			SDIP, QFP, LQFP, SSOP, SOP	One to four 8-bit, one or two 16-bit, one 18-bit, as many as eight PWMs, watchdog	One or two UARTS, synchronous serial I/Os, A9	15	As many as 16 channels, 8/16-bit		\$2.50
Up to 64-kbyte RAM	External 8-bit such as flash		128/208 QFP, 484BGA	Three 16-bit, 32-bit watchdog, can add timers	UART, can add (UART, SPI, I <sup>2</sup> C, HDLC), 56 to 228 parallel I/Os	12, can add more		As many as 40,000 on-chip programmable-logic gates, as many as 120 user-definable I/O pins	\$4.80 to \$18.75
64-kbyte flash (program or data), 16- plus 4-kbyte SRAM			80 PQFP, 100 $\mu$ BGA	Two 160-bit multi-function timers (PWM, capture/compare, prescale), 8-bit prescale, real-time, watchdog	Two full-duplex Ethernet, USB, GPSI, SPI, UART, more via software, 52 parallel I/Os	15	Eight channels, 10-bit		\$13.30
11- to 22-kbyte multiple-time programmable, 256- to 1024-byte SRAM			20 SO/ $\mu$ BGA	Four 8-bit	115-kbps UART, SPI, as many as 60 parallel I/Os	As many as 24, 16 events	13 channels, 12-bit	Prescaler, 1-Hz interrupt	\$2 to \$4
11- to 22-kbyte multiple-time programmable, 512- to 1024-byte SRAM			44/100 LQFP, 44 LPLL	Four 8-bit	115-kbps UART, SPI, as many as 60 parallel I/Os	As many as 24, 16 events	13 channels, 10/16-bit	Prescaler, 1-Hz interrupt	\$4 to \$8
8-kbyte	2 DMA, external flash		100 VQFP	Six programmable reload timers	Two UARTS, 32 parallel I/Os	32		Secure socket layer, Ethernet, and PPP-driver support	\$9.05
OTP, EPROM, 236-byte SRAM			18/28/40 DIP 18/28 SOIC, 20 SSOP 44 PLCC/QFP	Two or three 8-bit with 6-bit prescaler, watchdog	One UART, 32 parallel I/Os	Six	Eight channels, 8-bit	In-circuit programming, power-on reset, brownout reset	NA

## 16-BIT MICROPROCESSORS

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Fujitsu Microelectronics</b> www.fmi.fujitsu.com Enter No. 361	F2MC16L F2MC16LX F2MC16F	16 to 64	24/16, external: 8 or 16 (multiplexed)	16	1.8 to 5.5	125 mW (16 MHz)	Stop, sleep, subclock, hardware standby	Two 16-bit accumulators		
<b>Intel Corp</b> www.intel.com Enter No. 362	80C186EA/XL 80C188EA/XL	8, 12, 13, 20, 25	External 16/16	8, 16	5	100 to 105 mA	Power-save		Coprocessor	
	80C186EB 80C188EB	8, 13, 16, 20, 25	External 16/16	8, 16	5	115 mA	Idle, power-down		Coprocessor	
	80C186EC 80C188EC	13, 16, 20, 25	External 16/16	8, 16	5/3, 5.5 tolerant	125 mA	Idle, power-down, power-save		Coprocessor	
	MCS96/296	16, 20, 25, 40, 50	16 to 24/16	24	5	150 mA	Idle, power-down	Enhanced mathematics instructions		
<b>Mitsubishi Electric &amp; Electronics USA Inc</b> www.mitsubishichips.com/startMCU.html Enter No. 363	M16C	32 kHz to 20 MHz	20/16, external: 20/8 or 16	16	2.5 to 5.5	25 to 250 mW	Standby: 20 $\mu$ W, sleep: 0.5 $\mu$ W	16 $\times$ 16-bit multiply-accumulate instructions		
<b>Motorola Inc</b> www.motorola.com/semiconductors Enter No. 364	68HC12 family	8	16	16	3, 5	250 mW (8 MHz)	Wait, stop			
	68HC16 family	25	20/16	16	5	770 mW (16 MHz)	Wait, stop	Multiply-accumulate instructions		
<b>Ok! Semiconductor</b> www.okisemi.com Enter No. 365	MSM66573 family	14 to 30	20/8	8 to 32	2.4 to 3.6 or 4.5 to 5.5	36 mA	Stop, halt	Multiplier instruction		
<b>Philips Semiconductors</b> www.philips.semiconductors.com Enter No. 366	XA family	30 or 32	16	16	2.7 to 5.5	60 to 110 mA	Idle: 22 to 40 mA, power-down: 5 to 30 $\mu$ A	16 $\times$ 16-bit		
<b>STMicroelectronics</b> www.st.com Enter No. 367	ST10F269	40	Up to 24/16 demultiplexed (customizable)	16, 32	5	190 mA	Idle: 20 mA (plus the CPU clock frequency), power-down: 500 $\mu$ A	One-cycle multiply-accumulate instructions		
<b>Texas Instruments</b> www.ti.com/sc/msp430 Enter No. 368	MSP 430X1XX	Up to 8	16/16	16	1.8 to 3.6	250 $\mu$ A	Standby: 1 $\mu$ A, off: 0.1 $\mu$ A	One-cycle multiply, signed multiply, multiply-accumulate instructions, multiply-accumulate instructions		
	MSP 430X3XX	Up to 4	16/16	16	2.5 to 5.5	400 $\mu$ A/MIPS	Standby: 1.6 $\mu$ A, off: 0.1 $\mu$ A	One-cycle multiply, signed multiply, multiply-accumulate instructions, multiply-accumulate instructions		
	MSP 430X4XX	Up to 8	16/16	16	1.8 to 3.6	250 $\mu$ A/MIPS	Standby: 0.8 $\mu$ A, off: 0.1 $\mu$ A	One-cycle multiply, signed multiply, multiply-accumulate, multiply-accumulate		
<b>Toshiba America Electronic Components</b> www.toshiba.com Enter No. 369	TLCS900/H	8 to 25	24/16	8, 16, 32	3/5	69 mA	Run: 35 mA, idle2: 27 mA, idle1: 5 mA, stop: 0.5 $\mu$ A			

## 32-BIT MICROPROCESSORS

<b>Agilent Technologies</b> www.agilent.com/view/mobile Enter No. 370	AAEC-2000	200	32/32	16, 32	1.8/3.3	380 mW	Standby, sleep	32 $\times$ 32-bit multiply-accumulate instruction, DSP connectivity through synchronous serial port		16-kbyte instruction/data, 64-way set associative
<b>Alchemy Semiconductor</b> www.alchemysemi.com Enter No. 371	Au1000 Au1500	266, 333, 400, 500	32/32	32	1.25 to 1.8/3.3	900 mW to 1.2W	Idle, sleep	Multiply-accumulate instructions		16-kbyte instruction/data
<b>Altera</b> www.altera.com Enter No. 372	ARM-Based Excalibur	166, 200	16/via PLD	16, 32	1.8/2.5 to 3.3		Yes	32 $\times$ 8-bit, user-definable	Can be added	8-kbyte instruction/data

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
32- to 384-kbyte masked ROM, 128- to 512-kbyte flash, 640-byte to 16-kbyte RAM			64-120 QFP/LQFP/SQFP/SDIP (plastic)	16-bit, reload, PPG, PWM, 18-bit watchdog	Three serial I/Os, three CANs, five UART, as many as 102 parallel I/Os	16 external	Four/eight/16 channels, 10-bit	Five resets, LCD controller, stepper-motor controller	\$3 to \$14
			68 PLCC/PGA/JEDEC, 80 QFP/SQFP	Three 16-bit		Two internal, five external			\$3.90 to \$6.30
			80 QFP/SQFP, 84 PLCC	Three 16-bit	Two	As many as 129 external			\$5.05
			100 QFP(EIAJ)/PQFP/SQFP	Three 16-bit	Two	External (8259A)			\$8.81
8/16/32/56-kbyte EPROM, OTP, ROM, 232/488/744/1000/1500-byte SRAM			PLCC, QFP, SQFP, SDIP, CDIP	Two to four 16-bit, PWM, high-speed I/O	One or two UARTs	19 to 37	Eight channels, 10-bit	Motion control	\$4.39 to \$11
16- to 256-kbyte flash, OTP, mask, 3- to 20-kbyte SRAM	DRAM		80 to 144 QFP	11 16-bit, zero to two PWM, watchdog	As many as five UARTs, serial I/Os, USB, CAN, as many as 124 general-purpose I/Os	As many as 25 internal, eight external, four software, seven levels	As many as 26 channels, 10-bit, DAC	LCD, CRC, key-on wake-up	\$3 to \$15
32- to 128-kbyte flash, 1-kbyte SRAM			112 LQFP, 80 QFP	Eight-channel 16-bit, pulse accumulator	SCI, SPI, J1850, CAN, as many as 91 parallel I/Os	As many as 64	10-bit		\$6 to \$15
1- to 4-kbyte SRAM		Integrated	132 PQFP, 144 LQFP, 120/160 QFP	CTM7, general-purpose timer, two time-processor units	SCI, SPI, queued SPI, as many as 64 parallel I/Os	As many as 252	10-bit		\$6 to \$35
64-kbyte flash, 4-kbyte SRAM			100 QFP/TQFP	real-time, watchdog	27 internal, six external, nonmaskable	Eight 10-bit			\$5.50
256- to 2048-byte RAM			44 PLCC/LQF	Three (equivalent to 80C51 T0, T1, T2) watchdog	UART, SPI, I <sup>2</sup> C		8-bit		\$5.25 to \$10
256-kbyte flash, 12-kbyte SRAM		Yes	144 PQFP	Two units with five timers	Two CAN, synchronous/asynchronous, high speed	Eight channels, 16 priorities for 56 sources	16 channels, 10-bit	On-chip bootstrap loader and PLL	\$20.40
1- to 60-kbyte flash, up to 2-kbyte SRAM			20/28 SOIC/TSSOP, 64 QFP	16-bit watchdog, 16-bit PWM	USART, 48 parallel I/Os	All peripherals and I/O	12-bit		99 cents to \$5.95
16- or 32-kbyte OTP, 128-byte to 2-kbyte SRAM			48/56 SSOP, 64/100 QFP	Two 8-bit, 16-bit watchdog, 16-bit PWM	USART, 40 parallel I/Os	All peripherals and I/Os	14-bit		\$1.75 to \$6.95
4- to 60-kbyte flash, 256-byte to 2-kbyte SRAM			64/80/100 PQFP	Two 8-bit, 16-bit watchdog, 16-bit PWM	USART, 48 parallel I/Os	All peripherals and I/Os	12-bit		\$2.55 to \$6.95
Up to 256-kbyte ROM/flash, up to 8-kbyte SRAM	Yes		64 to 144 QFP/LQFP	As many as eight 8-bit, one or two 16-bit serial I/O	As many as three UARTs, synchronous	Nine CPU, 28 internal, 10 external, seven levels	As many as eight channels, 16-bit		\$5.75
External ROM, SROM, flash, burst flash, 40-kbyte SRAM	SDRAM, SRAM, flash, burst flash, ROM, SROM	64-entry TLB	256 PBGA	Three timers, real-time, dual PWM	Three UARTs, serial I/O, smart battery, smart card, USB, IrDA, 60 general-purpose I/Os	Eight user, 20 system		On-chip debug, AC'97 audio, LCD controller; separated advanced high-performance bus, PCMCIA, dc/dc converter	\$20
	Yes	Yes	324/424 PBGA		Two or four UARTs	Yes			\$39
256-kbyte, single-port SRAM; 128-kbyte, dual-port RAM	Single- and double-data TLB-rate SDRAM	Dual 64-entry 484 FBGA	1020 FBGA, 672 FBGA	32-bit, watchdog	UART, can add parallel	Can be added			NA

(con't on pg 44)

### 32-BIT MICROPROCESSORS (CONTINUED)

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Altera</b> www.altera.com Enter No. 372	Nios	80	17/16 or 33/32	16	1.8, 2.5/1.8, 2.5, 3.3, 5		Clock reduction via static design	Two-cycle 16×16-bit, 1-bit/clock, user definable	Can be added	
<b>AMD</b> www.amd.com Enter No. 373	ElanSC520	100, 133	PCI Revision 2.2	32	3.3/5 tolerant	1.6W			Yes	16-kbyte write-back
<b>ARC Cores</b> www.arccores.com Enter No. 374	Tangent-A4	User definable	32/32, addressing: 24/32 (user definable)	32	User definable	User definable	Sleep	16/24-bit and dual 16-bit multiply-accumulate, XY memory, modulo, bit-reverse, pre-increment, post-increment/two 32×32-bit options	Can be added	Up to 32-kbyte instruction/data, direct-mapped, two- or four-way set associative, line locking
<b>Fujitsu Microelectronics</b> www.fmi.fujitsu.com Enter No. 375	FR Series	25 to 66	32/32, external: 24/16	16	2.7 to 5.5	230 mW	Sleep, stop	DSP macro/32×32-bit with barrel shifter and bit search		1-kbyte instruction
<b>Hitachi Semiconductor</b> www.hitachi.com/semiconductor Enter No. 376	SH-2	50	16/32	16	3/4.5 to 5.5		Sleep, module-, software and hardware standby	Yes		
	SH-3	100 to 160	16/32	16	1.9/3.3	630 mW	Sleep: 248, standby: 0.05	Yes		16-kbyte mixed instruction/data, 16-kbyte XY DSP
<b>IBM</b> www.chips.ibm.com Enter No. 377	401GF	50	32/32	32	3.3	0.2W	Wait: 40 mW, doze: 30 mW, nap: 5 mW	32×32-bit		2-kbyte instruction, 1-kbyte data
	403GA 403GB 403GC 403GCX	25 to 80	32/32	32	3.3	0.51W	Wait: 30 mW, sleep: 0.1 mW	32×32-bit		2- to 16-kbyte instruction, 1- to 8-kbyte data
	405GP/CR	200 to 266	32/8, 16, 32	32	2.5/3.3	1.1W (200 MHz)		16×16-bit multiply-accumulate instructions/32×32-bit		16-kbyte instruction, 8-kbyte data
	440GP	400 to 500	32/8, 16, 32	32	1.8/2.5 or 3.3	3W (400 MHz)	Sleep: 1W	16×16-bit multiply-accumulate instructions/32×32-bit		32-kbyte instruction/data
	603eEM603e	100 to 200	64/32	32	2.5 or 3.3/3.3	4W	Doze: 1.5W, nap: 150 mW, sleep: 120 mW	32×32-bit, fixed-point	IEEE-754-unit compatible, single/double precision	16-kbyte instruction/data
	740 750 750CX 750CXe	200 to 700	64/32	32	1.8 to 3.1/1.8, 2.5, 3.3	6W (500 MHz)	Doze: 2.3W, nap: 250 mW, sleep: 200 mW	32×32-bit, fixed-point	IEEE-754-unit compatible, single/double precision	32-kbyte instruction/data
<b>IDT</b> www.idt.com Enter No. 378	RC32332 RC32334	100, 133, 150	23/32	32	3.3	1.5 to 1.8W	Wait	Four instructions		8/2-kbyte instruction/data, two-way set associative
	RC32355	133, 150	22/32	32	2.5/3.3	1.5W	Wait	Four instructions		8/2-kbyte instruction/data, two-way set associative
<b>Improv Systems</b> www.improvsys.com Enter No. 379	IWORX	90.44	Utopia, serial packet, controller interface	32	3.3 to 1.8	2.5W		Utopia bus		
	Jazz	Up to 200	16/32	32	User definable	20 mW	Halt, sleep, idle	DSP operations, saturation, bit-reverse/16×16-bit, 32×32-bit, custom operations	User definable	
<b>Infineon Technologies</b> www.infineon.com/tricore Enter No. 380	C166	16 to 40	24/16 and 32	16, 32	2.7 to 5.5	69 to 500 mW	Power-down: 10 mA, wakable: 140 mA, idle: 420 mA	16×16-bit and 32×16-bit		
	TC11IB	96	32	16, 32	1.8/3.3			Dual 16×16-bit multiply-accumulate units		32-kbyte instruction/data

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
ROM, 512-byte register file, 32-byte register window	SRAM, SSRAM, SDRAM, flash		TQFP, RQFP, PQFP, BGA, FBGA	PWM, watchdog, configurable	RS-232, SPI, Ethernet, general-purpose I/O, IDE, PCI, configurable	64			NA
	SDRAM		388 PBGA	Programmable-interval, general-purpose, software, real-time clock, watchdog	Two 16650 UARTs, synchronous serial, 32 parallel I/Os, PCI-bus Revision 2.2	22 levels		JTAG debug	NA
Up to 16-kbyte RAM, scratchpad				Two 32-bit, user-definable	As many as eight UARTs, optional parallel/JTAG port, user-definable	16 (three levels), as many as 16 more		Optional 10/100-Mbps Ethernet, Bluetooth	NA
Up to 512-kbyte flash, up to 128-kbyte SRAM	DRAM, DMA		100 QFP, 100 LQFP, 144/120/208 FBGA	Two 8-bit, UART/baud rate, 16-bit reload, free-running, PPG, PWM	Two serial I/Os, three CAN synchronous, as many as four UARTs, as many as 120 parallel I/Os	As many as eight external	Four/eight channels, 10-bit		\$5 to \$18
256-kbyte flash, 12-kbyte RAM			80/100 QFP	Two 16-bit, watchdog	Two or three serial I/O, 54 to 69 parallel I/Os	Five	12 to 16 channels, 10-bit		\$22 to \$23
SRAM/SDRAM/ROM interfaces	Yes	Yes	240 HQFP/CSP	Three 32-bit	Three serial I/Os, 104 parallel I/Os	11 external	Eight channels	USB, color-LCD controller	\$19.50 to \$22.50
				Four					\$6.20
	DRAM, DMA	64-entry TLB, variable page size		Four					\$11 to \$21
4-kbyte SRAM	SDRAM, DMA	64-entry TLB, variable page size		Four	General-purpose I/O			PCI, Ethernet media-access controller	\$23 to \$65
8-kbyte SRAM	DDR, SDRAM, DMA	64-entry TLB, variable page size		Five	General-purpose I/O			PCI-X, two Ethernet media-access controllers	NA
		128-entry two-way set-associative TLB, software reload		Two				Debugging support	\$18 to \$37
		128-entry two-way set-associative TLB, hardware reload		Two				Thermal-assist unit, debugging support, performance monitor	\$50 to \$210
	×32 SDRAM, 8/16/32-bit ROM/flash	32-entry TLB	208 QFP, 256 BGA	Three 24-bit	One or two 16550-compatible, 12 to 16 parallel I/Os	Four, more via parallel I/O		Two or three external devices via V2.1 PCI bridge, EJTAG debug	\$14 to \$16
	×32 SDRAM, 8/16/32-bit ROM/flash	32-entry TLB	208 QFP	Three 24-bit	Two 16550 compatible, USB 1.1, I <sup>2</sup> C, 36	Four, parallel I/Os more via parallel I/O		10/100-Mbps Ethernet port, 25-Mbps SAR, 8-Mbps TDM, EJTAG debug	\$22
Integrated RAM			35×35 mm	Available		Available			\$178
As many as four segmented SRAM ports per processor	Denali				Use shared-memory access with SRAMs	Multiple levels		Composer tool suite customizes instructions, datapaths, software-development tools	License
L7432- to 256-kbyte ROM, 64-kbyte OTP, 1- to 11-kbyte SRAM			80/100/144 PTQFP and PMQFP	Three to 16 16-bit, watchdog, baud-rate generator, PWM, real-time	Two to five serial channels; one to five ASC, SPI, I <sup>2</sup> C, CAN, USB	As many as 56	As many as 24 channels, 10-bit	36-channel capture/compare, CAN interface, bootstrap loader	\$2.50 to \$15
1.5-Mbyte eDRAM	EBU (PC100 support)	Yes	388 PBGA	Six 32-bit (usable as 8- and 16-bit)	PCI, Fast Ethernet, SSC/SCI, ASC (IrDA), 16×50, MMCI, 96 parallel I/Os				\$57

### 32-BIT MICROPROCESSORS (CONTINUED)

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Infineon Technologies</b> www.infineon.com/tricore Enter No. 380	TC1775	40	32	16, 32	2.5/3.3 to 5		Four	Dual 16×16-bit multiply-accumulate units		16-kbyte instruction, 32-kbyte scratch
	TriCore	Up to 200	32	16, 32	1.8	310 mW	Sleep: 42 mW, deep sleep: 13 mW (180 MHz)	Signed-fraction, modulo, bit-reverse, pre-increment/post-increment; saturation, rounding, truncation/via coprocessor		Up to 32-kbyte
<b>Intel Corp</b> www.intel.com Enter No. 381	80386DX	16, 20, 25, 33	32/32	32	5	300 mA				
	80386EX 80386EXTB	16, 20, 25, 33	32, external: 26/16	32	3.3 to 5	250 to 320 mA	Idle power-down			
	80486DX4 80486DX2	Up to 100	32/32	32	3.3/5 tolerant	IntelDX4: 825 to 1075 mA; IntelDX2: 318 to 395 mA	Stop; auto-halt/idle power-down		32, 64, 80-bit formats	8- or 16-kbyte instruction/data, write-back
	80486SX 80486GX 80486SX	Up to 33	32/32, 16 to 32/16 to 32	32	3.3/5 tolerant	220 to 289 mA, 180 to 220 mA	Stop clock, auto-halt power-down			8-kbyte instruction/data, write-through
	80960 CX	16 to 40	32/32	32	37016	1034 mA	Wait	Yes		1- to 4-kbyte instruction, 1-kbyte data
	80960 HX	25 to 80	32/32	32	3.3/5	1578 mA	Halt, wait	Yes		16/8-kbyte instruction/data
	80960JX 80960VH	16 to 100	32/up to 32	32	3.3/5 tolerant	480 to 690 mA	Halt	Yes		2- to 16-kbyte instruction, 1- to 4-kbyte data, stack frame
	80960SX 80960KX	16, 20, 25	32/16 or 32	32	37016	340 to 420 mA		Yes	SB/KB only	512-byte instruction
	Xscale architecture	400, 600, 733	64 ECC, 32 coprocessor interface	16, 32	1 to 1.5/3 to 3.6	1.3W	Idle, drowsy, sleep	One-cycle 16×32+40-bit multiply-accumulate instruction/32×32-bit		32-kbyte instruction/data, 32-way set associative
<b>Lexra Inc</b> www.lexra.com Enter No. 382	LX4189	266	32/32	32	1.2 (0.13 μm)	200 mW	Standby: less than 50 mW 32×32-bit	One-cycle 16×16-bit, two-cycle data		Up to 16-kbyte instruction/
	LX4380	Up to 420	32/32	32	1.2 (0.13 μm)	44 mW (0.13 micron)		One-cycle 16×16-bit, two-cycle 32×32-bit		0- to 64-kbyte instruction/data
<b>MIPS Technologies</b> www.mips.com Enter No. 383	4Kc, 4Kn, 4Kp	200	32/32	32	Process dependent	100 mW (0.18 micron)	0.2 mW (0.18 micron)	One-cycle 16×16-bit, 32×16-bit, two-cycle 32×32-bit, 34-cycle 32×32-bit (4Kp)		0- to 16-kbyte instruction/data
<b>Mitsubishi Electric &amp; Electronics USA Inc</b> www.mitsubishichips.com/startMCU.html Enter No. 384	M32R/E	32, 40	32/32, external: 22/16	16, 32	2.7 to 3.3/5			16×16-bit, 32×16-bit, 32×32-bit multiply-accumulate instructions		
<b>Motorola Inc</b> www.motorola.com/semiconductors Enter No. 385	603e PowerPC	100, 133, 200, 266, 300	32/32 or 64	32, 64	2.5/3.3	4W	Nap, doze, sleep	Single-precision multiply-add array way set-associative	NaN, zero, infinity, normalized	16-kbyte instruction/data, four-
	MPC7410	400, 450, 500, 533	32/32 or 64	32	1.8/1.8 to 3.3	5.3W	Nap, doze, sleep	Altivec: 128-bit vector unit	Three-cycle pipeline single/double-precision	L1: 32-kbyte instruction/data, backside L2: 512-kbyte, 1- or 2-Mbyte
	MPC7440 MPC7450	533 to 700	32 to 36/64	32	1.8/1.8 to 2.5	13.3 to 15.9W	Nap, doze, sleep	Altivec: 128-bit vector unit	IEEE-754 single/double precision	L1: 32-kbyte instruction/data, backside L2: 512-kbyte, 1- or 2-Mbyte
	MPC755	300, 350, 400	32/32 or 64	32	1.8/2/1.8 to 3.3	4W	Nap, doze, sleep		Three/four-cycle pipeline single/double precision	L1: 32-kbyte instruction/data, backside L2: 256-kbyte, 512-kbyte or 1-Mbyte

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
40-kbyte data SRAM	32-bit, glueless, burst mode		329 PBGA	Three 32-bit, 34×24-bit, 64×16-bit	CAN, SDLM, two SSC/SPIs, two ASCs, 11×16-bit parallel port	More than 100 interrupt-request modes	Dual, 16 channels, 8/10/12-bit	Prescaler, duty cycle, phase discrimination, digital PLL	\$35
Up to 32-kbyte SRAM in 8-kbyte increments		128-entry, four-way set-associative				256 native, 256 more with peripheral-control processor		Hardware emulation and debugging support, Level 3 emulation and debugging support	NA
			132 PGA/PQFP			Maskable, nonmaskable interrupt			\$5.90
	Refresh-control unit		100/132 PQFP, 144 TQFP	32-bit down-counter, watchdog	UART, serial I/O, three 8-bit general-purpose I/Os	10			\$6.50 to \$10
			208 SQFP, 168 PGA			Reset, maskable, nonmaskable interrupt			\$21
			168 PGA, 196 PQFP, 176 TQFP			Reset, maskable, nonmaskable interrupt			\$16.55 to \$28.75
	Yes		168 PGA, 196 PQFP			Eight, nonmaskable interrupt		Supervisor protection	\$25.46
2-kbyte RAM	Guarded memory unit		168 PGA, 208 PQFP	Two 32-bit		Eight, nonmaskable interrupt		Supervisor protection	\$34.60
1-kbyte RAM	SRAM, flash		132 PGA/PQFP, 196/324 PBGA	Two 32-bit	PC	Programmable high-speed controller		16/16 global/local 32-bit registers, high-bandwidth burst bus, JTAG	\$9.98 to \$44.20
	Yes		84 PLCC, 80 QFP, 132 PGA/PQFP			Four direct/handshake			\$7.98 to \$11.69
Up to 28-kbyte lockable cache	64-bit SDRAM with ECC, flash, three DMA	32-entry TLB	241 PBGA, 540 PBGA	Three 32-bit, six secondary PCI, four SDRAM	PC, eight general-purpose parallel I/Os; 66-MHz, 64-bit PCI-to-PCI bridge	Four external		JTAG debug, application-accelerator unit	
									License: \$350,000
		Two-entry, 4-kbyte page							License: \$568,000
Configurable	Optional			Optional				Fully synthesizable core	License
Up to 768-kbyte flash, up to 40-kbyte RAM			144 to 240 QFP, 255 FBGA	As many as 64 multifunction channels	As many as six serial I/Os, CAN, as many as 21×8-bit parallel	As many as 31 internal	As many as 32 channels, 10-bit	JTAG debug, wait controller	
		4-Pbyte virtual, 4-Gbyte physical	240 CQFP, 255 CBGA, 255 PBGA		Yes				
		128-entry, two-way set-associative, four block-address translation	360 CBGA/PBGA					Modified/exclusive/shared/invalid cache coherency, MPX bus, four-stage pipeline	\$58 to \$99
		128-entry, two-way set-associative, four block-address translation	360/483 CBGA					Modified/exclusive/shared/invalid cache coherency, MPX bus, four-stage pipeline	\$129 to \$300
		128-entry, four-way set-associative, four block-address translation	360 PBGA					Modified/exclusive/shared/invalid cache coherency, MPX bus, four-stage pipeline	\$45 to \$78

### 32-BIT MICROPROCESSORS (CONTINUED)

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Motorola Inc</b> www.motorola.com/ semiconductors Enter No. 385	MPC8245	266 to 300	32/32 or 64	32	2/3.3	2W			Yes	16-kbyte instruction/data
	MPC826X	100 to 266	18/32, external: 8 to 64 (configurable)	32	2.5/3.3; HiP4: 1.8/3.3	2.5W	Nap, doze, sleep, automatic for idle units		IEEE-754 compatible, single/double precision	16-kbyte instruction/data
	MPC8XX	50 to 80	32/32	32	3.3/5		Doze, sleep, deep sleep, power-down			Up to 16-kbyte instruction/data
<b>National Semiconductor Corp</b> www.national.com Enter No. 386	Geode family	200 to 333	64/64, external: PCI 32 (multiplexed)	8, 16, 32, 48	1.6 to 2/3.3	1.2W at 2V, 300 MHz (80% active idle)	Active idle: 0.6W, standby: 170 mW, sleep: 140 mW (1.6 V, 200 MHz)	8, 16, 32×8, 16, 32-bit multi-media-extension instructions	IEEE-754 compatible, single-precision, 64 or 80 bits	
<b>NEC Electronics</b> www.necel.com Enter No. 387	V850 family	20 to 50					Modes to turn clock off	One-cycle 16×16-bit, 32×32-bit multiply-accumulate instructions		
	VR4121	131, 168	32	32	2.5/3.3	270 mW	Standby, suspend, hibernate			16- to 32-kbyte direct-mapped instruction, 8-kbyte data
	VR4122	150, 180	64, external: 32/16	16, 32	1.8/3.3	350 mW	Standby, suspend, hibernate			32/16-kbyte instruction/data, direct-mapped
	VR4131	200	64, external: 32/16	16, 32	1.5/3.3	220 mW	Standby, suspend, exsuspend, hibernate	One-cycle 32×32+64-bit multiply-accumulate instructions		16-kbyte instruction/data, two-way set associative
	VR4181	66	64, external: 32/16	16, 32	2.5 or 3.3	150 mW	Standby, suspend, hibernate			4-kbyte instruction/data
<b>NetSilicon Inc</b> www.netsilicon.com Enter No. 388	NET+Works	33	16/32	32	3.3	300 mW		Yes		4-kbyte instruction/data
<b>Oki Semiconductor</b> www.okisemi.com Enter No. 389	ML670100	20 to 25	23/16	16, 32	2.7 to 3.6 or 3 to 3.6	60 mA	Stop, halt	Yes		
	ML671000	24	23/16	16, 32	3 to 3.6	70 mA	Stop, halt	Yes		
<b>picoTurbo Inc</b> www.picoturbo.com Enter No. 390	pT-100AX	200	32/32	16, 32	1.8 (0.18 μm)	0.45 mW/MHz		One-cycle multiply-accumulate instructions		
	pT-110AX	300	32/32	16, 32	1.8 (0.18 μm)	0.70 mW/MHz		Two-cycle pipeline multiply-accumulate instructions		
<b>PTSC</b> www.ptsc.com Enter No. 391	IGNITE I	100	32 (multiplexed)	8	3.3	166 mW	External variable-frequency clock	Yes	IEEE single/double precision	Four instructions per fetch
<b>Sharp Microelectronics of the Americas</b> www.sharpsma.com Enter No. 392	LH75400	50	16/24, 8/16, 16	16, 32	3.3	70 mA	Standby: 110 μA, stop: 90 μA	Yes		
	LH75401	50	16/24, 8/16, 16	16, 32	3.3	70 mA	Standby: 110 μA, stop: 90 μA	Yes		
	LH75410	50	16/24, 8/16, 16	16, 32	3.3	70 mA	Standby: 110 μA, stop: 90 μA	Yes		
	LH75411	50	16/24, 8/16, 16	16, 32	3.3	70 mA	Standby: 110 μA, stop: 90 μA	Yes		
	LH79520	75	26/32	32	1.8/3.3	70 mA	Standby: 40 mA, stop1: 320 μA, stop2: 5 μA	Yes		8-kbyte instruction, 8-kbyte data
	LH7A400	200	26/32	32	1.8	180 uA	Halt, standby: 20 μA	Yes		8-kbyte instruction, 8-kbyte data
<b>Tensilica Inc</b> www.tensilica.com Enter No. 393	Xtensa	320	32, 64, 128 customizable)	16, 24	1.5, 1.8, 2.5, 3.3	0.4 mW/MHz (0.18 micron)	Power-down, sleep, wait	Five Vectra DSP coprocessor options/16×16, 32×32	IEEE-754 compatible	0- to 32-kbyte instruction, 0- to 32-kbyte data, four-way set-associative

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
256-Mbyte ROM, 1-Mbyte to 2-Gbyte DRAM, one to eight banks of DRAM	Up to 2-Gbyte SDRAM		352 TBGA	Programmable interrupt controller with multiple timers and counters	DUART	Five hardware, 16 serial			NA
	12 memory banks	Separate units for cache, memory	480 TBGA	Four 16-bit (usable as two 32-bit)	Four serial communications controllers, three fast communications controllers, two multichannel HDLCs, four 120-bit general-purpose I/Os	37 sources		IMA, TC layer, and PCI	\$75.60 to \$135
	Eight memory banks, DRAM, SIMMs, SRAM, EPROM, flash	Separate units for cache, memory	256/357 LPBGA	Four 16-bit (usable as two 32-bit)	As many as four full-duplex serial communications controllers, two full-duplex serial management controllers, four 59-bit general-purpose I/Os	15 to 23 internal, seven or eight external		Simultaneous Ethernet/ATM, Utopia II multi-PHY/slave, background debug	\$16.13 to \$51.91
	64-bit SDRAM, 66- to 100-MHz, two 168-pin DIMMs, 512-Mbyte total							2-D graphics accelerator, display controller, PCI-host controller	\$25 to \$40
	SRAM, EDO DRAM, page ROM, SDRAM		100/144 LQFP, 100 QFP, 121/157 FBGA	8-bit, 32-bit, PWM, event counter	CSI/UART, CSI, UART, CSI/I <sup>2</sup> C	Maskable, external, software traps			
	66-MHz	32 double-entry TLB, 4-kbyte to 1-Gbyte page	224 FPBGA	Four 32-bit	115-kbps serial	Yes	Yes	Clock-generator unit	\$20 to \$25
	ROM, synchronous 66-MHz DRAM, flash	32 double entry TLB, 1 to 256-kbyte page	224 FBGA	Four 32-bit	115 kbps serial	Yes	Yes	Clock-generator unit	\$25 to \$30
	ROM, synchronous 100-MHz DRAM, flash	32 double-entry TLB, 1- to 256-kbyte page	224 FBPGA	Real-time	Two 16550-compatible, serial debug, synchronous three-line clock			Programmable clock management for each peripheral	\$25
	66-MHz, ROM, EDO-type DRAM, SDRAM, SROM, flash	32 double-entry TLB, 1- to 256-kbyte page	224 FBGA	Four 32-bit	115-kbps serial	Yes	Yes	Clock-generator unit	\$10 to \$15
	SRAM, SDRAM, DRAM		208 PQFP	Two	Real-time output ports	Four		Ethernet, HDLC, coprocessor interface	
4-kbyte SRAM			144 LQFP	Timebase, two PWM		19 internal, nine external	Eight 8-bit		\$6.50
4-kbyte SRAM	Two DMA (64-Mbyte)		128 QFP	Timebase, watchdog		13 internals, nine externals			\$5.50
	Optional picoPack		208 PQFP (test chip)	Optional picoPack		Optional picoPack			NA
1- to 64-kbyte instruction/data, direct-mapped, configurable	Optional picoPack		208 PQFP (test chip)	Optional picoPack		Optional picoPack			NA
	DRAM		100 PQFP	VPU	Hardware baud-rate generation	Eight levels			NA
16- plus 16-kbyte SRAM	External SRAM only		144 LQFP	Three 16-bit	Three UARTs, SPI, CAN 2.0b, 68 parallel I/Os	Seven external	Eight 10-bit		\$7.60
16- plus 16-kbyte SRAM	External SRAM only		144 LQFP	Three 16-bit	Three UARTs, SPI, CAN 2.0b, 68 parallel I/Os	Seven external	Eight 10-bit		\$8.60
16- plus 16-kbyte SRAM	External SRAM only		144 LQFP	Three 16-bit	Three UARTs, SPI, 68 parallel I/Os	Seven external	Eight 10-bit		\$6.60
16- plus 16-kbyte SRAM	External SRAM only		144 LQFP	Three 16-bit	Three UARTs, SPI, 68 parallel I/Os	Seven external	Eight 10-bit		\$7.60
32-kbyte SRAM	SRAM/ROM/flash/SDRAM	WinCE enabled	176 TQFP	Four 16-bit	Three 16550 UARTs, SPI, Microwire, TI's SSI, 64 parallel I/Os	Six			\$10
80-kbyte dual-ported SRAM (CPU and LCDC)	SRAM/ROM/flash/SDRAM/flash/SROM	WinCE enabled	256 PBGA	Three 16-bit, two PWM, watchdog, real-time clock	Three UARTs, SPI, MicroWire, SSI, AC'97, 64 parallel I/Os	Eight			\$19
Up to 128-kbyte ROM, up to 256-kbyte RAM		Optional		Three 32-bit		32			License

### 32-BIT MICROPROCESSORS (CONTINUED)

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>Toshiba America Electronic Components</b> www.toshiba.com Enter No. 394	TMPR 1940 CYAF	32	32, external: 8 or 16	16, 32	2.7 to 3.6	165 mW (ROM)	Stop, sleep, slow	One-cycle multiply-accumulate instructions		
	TMPR 1940 FDBF	32	32, external: 8 or 16	16, 32	2.7 to 3.6	280 mW	Stop, sleep, slow	One-cycle multiply-accumulate instructions		
	TMPR 3911BU 3911BxB	58.9	32	32	2.6/3.3	150 mW	Doze, sleep	One-cycle 32× multiply-accumulate instructions		4/1-kbyte instruction/data, direct-mapped, two-way set-associative
	TMPR 3912AU-923912 XB-92	92	32	32	3.3	360 mW	Doze, sleep	32×32+64-bit multiply-accumulate instructions		4/1-kbyte instruction/data, two-way set-associative
	TMPR 3922CU	129	32	32	2.7/3.3	500 mW	Doze, sleep	One-cycle 32× 32+64-bit multiply accumulate instructions		16/8-kbyte instruction/data, two-way set-associative
	TMPR 3927BF	133	32	32	2.5/3.3	1W	Reduced frequency, doze, halt	32×32+64-bit		8/4-kbyte instruction/data, two-way set-associative
<b>Transmeta Corp</b> www.transmeta.com Enter No. 395	Crusoe TM5800 TM5500	Up to 800	32	32	0.9 to 1.3	1W	Auto-halt, quick start, deep sleep	Yes	Yes	L1: 64-kbyte instruction, 64-kbyte data, L2: 512-kbyte
<b>Triscend</b> www.triscend.com Enter No. 396	A7 configurable family	Up to 60	32, external: 20 to 32/ 8 to 32	16, 32	2.5/2.5 to 3.3	1.65W	Power-down, selective disable	32×32+64-bit multiply-accumulate instructions/ 32×8-bit, options available		8-kbyte unified cache
<b>Xilinx</b> www.xilinx.com Enter No. 397	MicroBlaze	125	32	32				User-definable DSP/two-cycle 32×32-bit multiply		

### 64-BIT MICROPROCESSORS

<b>MIPS Technologies</b> www.mips.com Enter No. 398	20Kc	400 to 600	Definable	32	1.5 to 1.8	3.1 mW/MHz	Yes	32×32-bit, 32×64-bit, 64×64-bit	64-bit paired-single and MIPS-3-D	0- to 64-kbyte instruction/data
	5Kc	200 to 250	Definable	32	1.5 to 1.8	1 mW/MHz		32×32-bit, 32×64-bit, 64×64-bit	Optional	0- to 64-kbyte instruction/data
<b>NEC Electronics</b> www.necel.com Enter No. 399	VR4310	133, 167	64, external: 32	32	3.3	1.2 to 2.5W				16-kbyte instruction, 8-kbyte data
	VR5000	200, 250	64, external: 64	32	3.3	5W	Standby	32×32- and 32×16-bit multiply accumulate instructions	IEEE-754, 32 and 64 bit	32-kbyte instruction/data, two-way set-associative
	VR5432	167 to 200	64, external: 32	32	2.5/3.3	1.8W		32×32+64-bit multiply-accumulate instructions, barrel shift	IEEE-754, 32 and 64 bit	32-kbyte instruction/data, two-way set-associative, line locking
	VR5500	300	64, external: 64 (32 option)	32	1.5/3.3	1.5W		Multiply-accumulate unit	IEEE-754, 32 and 64 bit	32-kbyte instruction/data, two-way set-associative, line locking
<b>PMC-Sierra MIPS Processor Division</b> www.pmc-sierra.com Enter No. 400	RM5200	250, 300, 350	32/64	32	1.65, 1.8/ 2.5, 3.3	Less than 1W (400 MHz)	Standby	Multiply-accumulate unit/integer DSP multiply-accumulate instructions integer DSP multiply-accumulate instructions, multiply (three-operand and cycle)	One/two-cycle rate single/double precision	32-kbyte instruction/data, two-way set associative
	RM7000	300, 350, 400, 450, 500, 550, 600	64	32	1.8, 1.5, 1.2/3.3, 2.5, 1.5	4W (400 MHz)	Standby	Integer DSP multiply-accumulate instructions/integer DSP multiply-accumulate instructions, multiply (three-operand and -cycle)	Single/double precision	16-kbyte instruction/data, L2: 256-kbyte, four-way set-associative, line locking, write back/through
	RM9000X2	1000	64/8, local bus: 8, 16, 32	32	1.2, 2.5, 3.3	5W		Yes	IEEE-754	16-kbyte instruction/data, L2: 256-kbyte four-way set-associative

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
256-kbyte mask ROM, 10-kbyte SRAM			100 LQFP	Four 16-bit, four 8-bit, watchdog	Four UART/serial I/Os, I <sup>2</sup> C bus/serial I/O, 77 parallel I/Os	12 external, nonmaskable interrupt			
512-kbyte flash, EEPROM, 16-kbyte SRAM			100 LQFP	Four 16-bit, four 8-bit, watchdog	Four UART/serial I/Os, I <sup>2</sup> C bus/serial I/O, 77 parallel I/Os	12 external, nonmaskable interrupt			
	SDRAM, DRAM, SRAM, ROM, flash	32-entry, 4-kbyte pages	176 LQFP, 177 BCSP	Real-time clock, watchdog	Concentration-highway interface, UART, IrDA, SPI, 39 parallel I/Os	As many as 39 external		Codec interface (soft modem, voice recognition/synthesis)	\$10
	SDRAM, DRAM, SRAM, ROM, flash	32-entry, 4-kbyte pages	208 LQFP, 217 FBGA	Real-time clock, watchdog	Concentration-highway interface, UART, IrDA, SPI, 39 parallel I/Os	As many as 39 external		Codec interface (soft modem, voice recognition/synthesis)	\$18
	SDRAM, DRAM (EDO), SRAM, ROM, flash	4-kbyte to 4-Mbyte, 64-entry pages	208 LQFP	Two, watchdog	Concentration-highway interface, UART, IrDA, SPI, 48 parallel I/Os	As many as 48 external		Companion chip TC6358TB	\$28
	SDRAM, SGRAM, DIMM flash, SMROM, SRAM, ROM	4-kbyte to 4-Mbyte, 64-entry pages	240 PQFP	Three	Two UARTs, 16 parallel I/Os	Six external		Debug-support unit	\$20
	64-bit DDR, SDR	Yes	474 BGA						\$85 to \$200
4k×32-bit (upper half optionally used as trace buffer)	8-, 16-, or 32-bit SRAM, flash, SDRAM, four DMA	Eight protected, cacheable, resizable memory regions	128 LQFP, 208 QFP, 280/484 BGA	Two 16-bit, 32-bit watchdog, can add timers	Two 16C550-compliant, can add HDLC, SPI, I <sup>2</sup> C; 83 to 189 parallel I/Os	15, can add more		As many as 40,000 on-chip programmable-logic gates, as many as 120 user-definable I/O pins	\$19.95
72 to 3456-kbyte			Virtex/E, Spartan-II, Virtex-II	CoreConnect-enabled timer/counters, watchdog	CoreConnect-enabled UART, I <sup>2</sup> C, general-purpose I/O	CoreConnect-enabled controller			
	Optional	4-kbyte to 16-Mbyte, 48-entry page						Hard core	License
	Optional	4-kbyte to 16-Mbyte, 48-entry page						Coprocessor interface, fully synthesizable core	License
	Use 4375 or third party	32 double-entry TLB, 4-kbyte to 16-Mbyte page	120 QFP	32-bit		Yes	Yes	Clock-generator unit, JTAG, sync interface	\$10 to \$15
	83/100-MHz	48 double-entry TLB, 4-kbyte to 16-Mbyte page	223 BPGA			Yes		Dual-issue superscalar, L2 cache interface	\$10 to \$15
	83/100-MHz	48 double-entry TLB, 4-kbyte to 1-Gbyte page	208 PQFP	Two 32-bit				Dual-issue superscalar, JTAG, N-Wire/N-Trace, 32/64-bit SysAD bus	\$20 to \$25
	133-MHz	48 double-entry TLB, 4-kbyte to 1-Gbyte page	272 BGA	Two 32-bit				Dual-issue superscalar, JTAG, N-Wire/N-Trace, 32/64-bit SysAD bus, ×2 to ×5.5 clock	\$35
	48 dual entries map 96 pages (4-kbyte to 16-Mbyte)		128/208 QFP			Optional exception vector			\$15
		64 dual-entry TLB maps 128 pages	256/304 BGA			10 external, nonmaskable interrupt			\$100
8-kbyte scratch RAM linear address mapping	DDR, SDRAM, 200-MHz DDR, DMA	64 dual entries, 4-kbyte to 256-Mbyte page	656 SBGA			10 external, nonmaskable interrupt, 256 levels, intra-CPU		Ability to put DMA packet headers into L2 while putting the remainder of the packet into main memory	NA

## 64-BIT MICROPROCESSORS (CONTINUED)

Company	Device family or device	CPU frequency (MHz unless otherwise noted)	Bus interface (address/data) (bits)	Instruction width (bits)	Operating voltages (V)	Typical power at maximum frequency	Power-down modes	DSP/multiplication hardware support	FPU	Caching
<b>SandCraft</b> www.sandcraft.com Enter No. 401	SR70000	600 to 800	64	64	1.5/3.3	5W (600 MHz)		Multiply-accumulate instructions/single- and double-precision operations	IEEE-754 compatible, decoupled from integer pipeline	L1: 32-kbyte instruction/data, four-way set-associative, L2: 512-kbyte, L3: 2- to 16-Mbyte
<b>Sun Microsystems</b> www.sun.com/microelectronics Enter No. 402	UltraSPARC IIe series	400, 500	64 with ECC, external: PCI 32	32	1.5/3.3	10W	Full, 1/2, 1/6th frequency with SDRAM self-refresh	32×32-bit, 64×64-bit, 128×128-bit	IEEE 754-1985 single/double precision, 1596.5-992 quad precision,	16-kbyte instruction/data, two-way set-associative, indexed/tagged, write-through, direct-mapped, L2: 256-kbyte
<b>Toshiba America Electronic Components</b> www.toshiba.com Enter No. 403	TMPR 4927TB	200	64, external: eight-channel bus controller	32	1.5/3.3	1.2W	Halt	One-cycle 64×64 multiply-accumulate instructions	IEEE-754 compliant, single/double precision	32-kbyte instruction/data, four-way set associative, FIFO, lock
	TMPR 4955AF-200	200	32	32	1.5/3.3	450 mW	Halt, doze	One-cycle, 64×64-bit multiply-accumulate	IEEE-754 instructions compliant, single/double precision	32-kbyte instruction/data, four-way set associative, FIFO, lock

Memory	Memory controller	MMU	Package selection	Timers	Serial, parallel I/O	Interrupts	ADC/DAC	Additional features	Price (10,000)
		TLB, 4- to 356-kbyte page				10 extended			NA
	64-bit SDRAM interface, four DIMMs, up to 2-Gbyte	Dual 64-entry, 8- to 4096-kbyte page	Socketable 370 ceramic PGA	Two 63-bit	32-bit, 66-MHz, 3.3V PCI 2.1-compatible, four general-purpose I/Os	As many as 48		Energy Star power management	\$145 to \$225
	Four-channel SDRAM	48-entry, fully associative TLB	420 TBGA	Three	Two serial, as many as 16 parallel I/Os	12 internal, six external		EJTAG debug	NA
		48 double-entry TLB	160 QFP					EJTAG debug	\$17