16-Gbit MLC NAND flash weighs in
Young Choi, Semiconductor Insights - July 30, 2007

To meet increasing demand for more digital storage, leading flash memory manufacturers are touting their latest single-chip 16-Gbit MLC NAND flash devices. Earlier this year, Toshiba announced a 16-Gbit MLC NAND flash manufactured in the 56-nm process node. Samsung, meanwhile, introduced a 16-Gbit MLC NAND flash using a 51-nm process, a half a process node ahead of Toshiba's.

Developing MLC NAND flash memories within the 50-nm range process node requires overcoming many technical challenges, from both a process and circuit design perspective. Some of the issues that must be addressed are the proper layout design of bitlines and surrounding dummy patterns; the placement of P-well bias; efficient self-boosting circuitry for row decoder and wordline switches; efficient and reliable high-voltage pump circuitry; and efficient read, programming, erase and verify algorithms to guarantee reliable operations with reduced charges stored in smaller flash memory cells.

Semiconductor Insights has analyzed the latest 16-Gbit MLC NAND flash devices from both Toshiba and Samsung. Initial results showed that both devices achieved impressive die area and Mbit/mm ratings for storage with some architectural changes from previous designs. More details of the new designs will be disclosed after further analyses of the architecture and circuits, process and device characteristics, and waveform analysis to show the innovations Samsung and Toshiba have made.

Samsung 16-Gbit NAND
In its latest 16-Gbit MLC NAND flash device, Samsung has simplified the floor plan and architecture from the previous-generation 65-nm 8-Gbit MLC NAND flash device. There are two row decoder areas, which split the memory array into four 4-Gbit arrays. Page buffers are now all consolidated in one side of the chip, as opposed to having two halves on either side of the memory array in the previous-generation product.
Samsung still has the bonding pads on both sides of the chip, but the 16-Gbit device has pads on both edges in the wordline direction, apparently to improve power distribution. The previous generation has pads in the bitline direction.

**Toshiba 16-Gbit NAND**
Toshiba's latest device has the same overall architecture and floor plan as its previous-generation 70-nm 8-Gbit MLC NAND flash. The page buffer size has been increased to 4 kbytes from 2 kbytes. The chip has two 8-Gbit flash memory arrays divided by row decoders.

As with the preceding device, all bonding pads are in one side of the chip. Toshiba appears to have a different architecture in its 8-Gbit manufactured in the same 56-nm process node. According to an "IEEE Journal of Solid-State Circuits" paper published in January, the 8-Gbit design appeared to have 4 kbytes of page buffers located between two 4-Gbit flash memory arrays. In 16-Gbit design,
However, the page buffers are along the side where the bonding pads are, and the row decoders are between two 8-Gbit arrays. By placing row decoders, page buffers and all bonding pads on one side, the latest Toshiba 16-Gbit device achieved efficient floor plan with only 173 mm$^2$ of chip size. Toshiba apparently has overcome challenges with internal power distribution and stability by putting all power pads on one side of the chip.

By migrating their production to 5x-nm process node, both Samsung and Toshiba have achieved 40 percent improvement of Mbit/mm$^2$ with only a 20 percent increase in chip size from their previous 8-Gbit designs. Samsung's design appears to have achieved about a 5 percent smaller chip size due to its smaller feature-size advantage over Toshiba.

<table>
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<th>Part number</th>
<th>Toshiba</th>
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</table>

(Click on image to enlarge)

**Road map to more bits per cell**

While flash makers continue to develop more advanced flash technology beyond 40 nm and 30 nm, increasing bit density by enhancing MLC technology to 3 bits per cell is being pursued at the 5x-nm process node. Toshiba and SanDisk are reportedly developing 3-bit-per-cell technology at their 56-nm process node to develop a 24-Gbit flash memory device. The 3-bit MLC technology will also produce 48-Gbit MLC NAND flash memories in the 40-nm generation.

Precise placement of eight unique threshold voltages to the flash memory cells and performing error correction would be challenges for developing 3-bit technology. The 4-bit technology is expected to emerge at the 40-nm process node. MLC technology for 3 bits per cell and 4 bits per cell is expected to be critical for companies to remain competitive in 2009 through 2011.

**Other challenges**

Availability of single-chip 16-Gbit MLC NAND flash memory devices is expected to stimulate the market for applications such as solid-state disk and hybrid hard drive. Samsung has announced a 64-Gbyte SSD using the latest 51-nm 8-Gbit SLC flash devices (equivalent to 16-Gbit MLC). Intel, for its part, has its Turbo Memory support for Windows Vista. SSD's faster boot times and application startup times, and its enhanced reliability and battery life, should spur the adoption of SSDs and HHDs in the notebook market.

With more opportunities come additional challenges for NAND flash memory, however. An interface standard and improved interface speed are required to increase design time and enhance overall
Efforts are being made to address these issues. Higher-density MLC NAND flash with more page buffers helps improve performance. This leaves the interface speed as more of an issue for overall performance improvement. Managing MLC NAND architectures from different manufacturers is another concern.

Open NAND Flash Interface is trying to address this issue with an industry-standard interface. ONFI has laid out an interface road map for reaching 400 Mbytes/second by adopting DDR DRAM techniques. About 30 companies have joined the ONFI camp, including Micron, Hynix and STMicroelectronics. (Toshiba and Samsung are not members.)

Another new interface technology is Mosaid's HyperLink NAND, targeting the SSD market. HLNAND addresses the MLC NAND flash management issue and interface performance enhancement by adopting a daisychained serial DDR interface.

It's still unclear whether these industry-standard efforts or any proprietary interface will prevail. Backward-compatibility issues might force them to target new applications. These initiatives could help establish a unified interface for application and system developers or cause further segmentation.

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