A methodology for IC power grid design

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Power supply noise and related issues have become critical for designs at 90nm and below due to the combination of several factors. Timing slowdown and functional failures are becoming common in these designs due to the power grid noise. However, physical design and verification methodologies have not sufficiently evolved to adequately address these power supply noise issues.

Planning, resource allocation, and design of a chip's power supply, which includes package, decoupling capacitance, and power grid network, have to be done in a holistic manner along with sign-off quality verification and analysis. Designers need techniques to reduce the dynamic voltage drop (DvD) in a design and its impact on timing and functionality, and they need to adopt a power aware physical design methodology.

Dynamic power grid noise

Power supply noise has the following components: resistive network drop, capacitively coupled power grid noise, and inductive element induced noise. The level of power supply noise and its impact on performance are being exacerbated by the technology and design trends.

Figure 1 illustrates average current and di/dt value projections based on the ITRS data [1]. The trend indicates that dynamic voltage drop from the simultaneous switching of devices is going to get worse in advanced technology nodes. Not only will a higher di/dt lead to a larger dynamic drop, but also, higher switching currents flowing in the wires will cause larger resistive drops.
Higher cell placement densities, shorter edge rates, and faster clock periods, as illustrated in Figure 2, will lead to more cells switching closer together, temporally and spatially, raising the demand for instantaneous current. Existing methodologies and design practices that address package design, on-die power grid sizing, and decoupling capacitor allocation will be inadequate in creating a power supply system capable of responding to larger and more frequent on-die current spikes that will be seen in next generation designs.

As designs migrate from the 130nm technology node, designers are looking beyond traditional static
voltage drop analysis to a full-chip dynamic simulation approach that considers the interplay of simultaneous switching current with the inductive and capacitive elements present in a design. One early form of dynamic analysis had involved partitioning the simulation cycle into several intervals and performing static analysis in each of the intervals.

Today, this method has been replaced by a highly accurate full-chip transient simulation solution that provides a complete picture of the dynamic voltage profiles in a design. This simulation technique considers resistive, inductive, and capacitive elements from the chip package and on-die grid, the dynamic current drawn by simultaneously switching outputs, and the capacitive loads present in the design. Figure 3 illustrates the simulation framework modeled in this solution.

![Dynamic simulation model](image)

**Figure 3 — Dynamic simulation model**

**Impact of dynamic power supply noise**

Static timing tools do not account for the impact to slack and slew from DvD, which is often much larger than the static voltage drop budget. The propagation delay of cells increases in the presence of power grid noise.

Additionally, gates in advanced processes are more likely to get affected from DvD. A combination of heightened gate delay sensitivity and increased power grid noise result in frequency slow-down in chips that otherwise pass static timing analysis. Many designs, especially those in 90nm nodes, have exhibited failures from dynamic voltage drop related issues.

The impact on timing will be even greater on the clock network where the buffers are often placed close to each other and switch together. The variability in power grid noise translates into increased skew resulting in failed hold time requirements. Timing and clock skew analyses have to take into consideration the dynamic voltage drop seen by the instances in the critical paths or by the buffers in the clock network.

Power grid noise also impacts the cross-talk immunity of a design. Cells are more likely to fail from coupling noise when they simultaneously experience a voltage drop and/or a ground bounce. Library characterization of cells often do not account for transient voltage drops and their impact on cells’ performance. Thus, functionality may be compromised, especially when the dynamic voltage drop is sustained over a period of time.

**Fixing power grid noise**

Designers have to estimate and compensate for power grid noise to ensure proper operation of their
circuits and to prevent failures from the sources mentioned earlier. The conventional technique has been to over-design the power supply network and to populate all available areas with decoupling capacitors. This approach has served reasonably well for previous generation of designs with higher noise margins and larger design guard bands.

However, with advanced processes, designers no longer have the luxury of padding their design targets and adding generous margins. Tighter design specifications including lower supply voltage and faster clock frequencies leave far less room for error. Time to market critical designs can afford only very few tape-out iterations before going to production.

Low cost designs are significantly impacted by over-designed power grids and greater use of silicon resources. Multiple debug and tape-out cycles are needed to identify and fix power grid related chip failures. Over-design of a power grid can also affect the project schedule, as routing and timing convergence becomes more difficult from the lack of available routing space.

Power grid design is traditionally based on heuristics or experience. The power networks are typically uniform in width and pitch across a design. Once designed, the power routes remain unchanged unless voltage drop verification performed prior to tape-out indicates problem areas. The problems with this approach are:

- The grid is not optimized for a particular design and its power consumption.
- The grid is uniformly over or under-designed.
- Issues with the power grid are addressed only late in the design cycle.

Intentional decoupling capacitance (decap) placement is also ad-hoc and does not help to suppress the power grid noise. These decap cells are usually placed in empty cell rows, where there is insufficient switching for them to be effective. In addition, indiscriminate decap placement can adversely affect a design through the consumption of more leakage current, which is a concern given that about 30% of a chip's total power in 90nm designs will come from leakage current.

**Power aware physical design**

Power aware physical design necessitates a change in current design practices. The initial power grid should be designed to meet certain specifications. A prototyping solution that can quickly generate multiple power grid designs for various user-defined constraints, such as different floorplan or power consumption scenarios, should be used to estimate the routing resource requirements.

The selected prototype grid should be optimized during the early parts of the design process, when there is still flexibility to change the power routes. A sign-off quality power grid analysis solution should be used to verify the quality of optimizations.

At a later stage of the design, when the placement is more defined, targeted fixes should be performed to the power grid to resolve voltage drop issues. Decoupling capacitance advisory should be automatic to address dynamic hot spots and enable designers to place decaps in a targeted manner, optimizing the dynamic voltage drop while minimizing the impact on decap leakage current.

Figure 4 shows a power aware physical design flow that provides a prototyping solution for the initial P/G route definition, allows for the optimization of the P/G grid along the design cycle, fixes P/G grid issues, advises on decap requirements, and places decaps in a targeted manner.
Grid prototyping

Grid prototyping should allow designers to explore different power grid design options for various design scenarios. An efficient, fast, and accurate power grid prototyping solution would allow designers to experiment with different floorplan options, multiple power consumption scenarios, and several routing budgets. The prototyping solution should be flexible enough to work in very early stages of the design, when minimal placement information is available, or in slightly more defined phases of the design, when early placement information and the scope for defining the global and local power grid are available.

The grid prototyping should be constraint driven to meet user-defined dynamic and static voltage drop targets while meeting specific routing resource usage restrictions. The multi-layer power grid generated by a prototyping solution should honor blockages and electromigration limits, explore pad placement options, and generate rings if needed.

It should give the users capabilities to explore non-uniform grid options wherein the high power regions get a higher share of the power grid resources. The prototyping solution should also have a fast turn-around time to enable multiple iterations.

Figure 5 shows how a design team can explore different power grid structures for different floorplan and power consumption scenarios. By performing this exercise, the design team can obtain an engineered estimate of the P/G grid routing resources that are needed for each scenario. They can then choose the power grid which best fits their most likely design scenario. This chosen grid will be optimal to meet their power and routing targets.
Power grid optimization and fixing

As the design evolves, the prototype grid should be optimized to reflect the design changes. To meet the designs' voltage drop targets, an optimization solution should redefine the grid by following user provided restrictions such as pitches and track requirements. This approach would allow designers to meet their voltage drop budgets through an automated process of refining their power grid. For a given voltage drop budget, the optimization solution would size wires to minimize the metal routing usage for the P/G grid. Instead of designing a grid first and then getting a voltage drop number, designers would fix the drop budget first and design a grid towards that budget.

Power consumption in a design, especially power density, is usually very non-uniform as seen in figure 6. The power density "hot-spots" are often present in the areas where clock buffers are inserted.
A clock instance power map, illustrated in figure 8, shows a close correlation with the power density map in figure 7. A power grid optimization solution should allocate more metal resources to areas that are likely to have higher voltage drop than to areas with sparse cell placement. This holds true especially for a flip-chip design where the power supply and distribution problems are more localized, compared to a wire-bond packaged design.
Once detailed placement is completed and timing optimization is ongoing, a global optimization of the power and ground networks is no longer feasible. In such cases, targeted fixes need to be done to the power grid to address the voltage drop "hot spots." The power grid should be widened only in hot-spot areas and shrunk in other areas, without compromising the total voltage drop.

The solution should provide a quick turn-around time for fixing P/G problems that may arise from design iterations. The users should be able to fix only specific areas in their designs, limit the fix to certain metal layers, and define the manner in which the fix can be done.

Figure 8 illustrates how a design's power grid would change after running an automated fix solution. The left panel shows the original uniform grid while the right panel shows the fixed grid where some wires have been widened while others have been shrunk.
Decap advisory and fix

Decaps serve as local reservoirs of charge, and their placement should be done in a targeted manner to reduce the power and ground noise to acceptable limits. However, ad-hoc sprinkling of decaps adds unnecessary leakage current while being ineffective in reducing the dynamic voltage drop. Increase in the resistive drop along power and ground lines necessitate the placement of decaps closer to the switching areas.

Designers should be guided to locations where decap placement would be most effective, and they should have the capability to automatically redefine the cell and decap placements to reduce DvD. A high voltage drop region does not necessarily have to be redesigned unless it affects the timing of paths that go through that region or affects the functionality of the cells in that region. Thus, a fixing solution should be based on an accurate dynamic power analysis with feedback to timing analysis, and should identify areas that need fixing using decap placement or wire resizing.

The decap placement solution should work both in an advisory mode, providing feedback to the designers about where decaps are needed, and also in a repair mode by placing decaps in legalized placement areas. It should meet user specified targets while honoring constraints such as total leakage current and placement restrictions.

It should provide the option to fix problems by using wire changes or decap placement or both based on the users' specifications. Figure 9 illustrates the voltage noise at the power supply node of an instance following two different decap fixing runs with different targets for reducing dynamic voltage noise.
Conclusions

The shortening of product life cycles has accelerated the introduction rate of new designs. Being first to market significantly impacts a product’s chances of success in this environment.

The high price of mask sets and the costs associated with frequent design changes require design teams to anticipate and address causes of failure in their designs. They have to look beyond traditional power grid design and analysis techniques to estimate and to reduce the impact of P/G noise on design timing and functionality.

Power grid noise is most commonly cited as the failure source in many failed 90nm designs. Other design teams have found P/G noise to manifest more subtly through issues such as loss in yield. A holistic approach to power supply design to address these concerns is required for next generation chips in which over-design and guard-banding are no longer viable options.

This article gave an overview of a power aware physical design methodology that will allow engineers to design a chip power supply to help mitigate P/G noise induced design failures and avoid late design changes. It highlighted data generated using a commercially available solution that integrates power grid prototyping, optimization, fixing and verification for dynamic power grid noise for faster and effective design closure.

References


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