M-LVDS receivers keep it safe with multi-level fault detection

Jim Dietz, Manager, New Product Development, Texas Instruments - March 30, 2005

Designers have long known the benefits of using low voltage differential signaling (LVDS) in diverse applications such as wireless basestations, projection TVs, plain-paper copiers and handheld consumer electronics. LVDS provides high speed signaling with low electromagnetic emissions and very low power consumption. However, the TIA/EIA-644A standard provides no guidance on how to deal with failsafe. Application-specific design requirements often demand deterministic outputs during line fault conditions or when LVDS drivers are inactive.

Various vendors supply an assortment of failsafe approaches and recommendations. Some approaches rely on added circuit components to provide known outputs with no input, external to line receivers. Other suppliers integrate circuitry to establish an internal bias, or detect input loss and force a fixed output. While each failsafe approach has its advantages, lack of standardization leads to interchangeability concerns. M-LVDS receivers address these shortcomings with an integrated failsafe solution, which is part of the TIA/EIA-899 standard.

M-LVDS receivers detect conditions including open-circuit, short-circuit, line disconnect and disabled drivers. This failsafe approach also provides the desired benefit of working over the full receiver input range, a common shortcoming of some previous solutions.

Who needs failsafe?

When synthesizing a data transmission system, designing for failure or non-operating conditions is often not the first concern. Speed, power, robustness and cost should be the first considerations. The designer will, however, eventually start to contemplate what happens when not all things operate as usual. "What will my receiver do when a cable is disconnected?" (the open-circuit problem); "What happens when my bus lines are shorted together?" (the short-circuit problem); "What will the receiver output go to when the driver (or drivers) are disabled?" (the idle-line problem); and "What will cause my receiver output to oscillate?" (the ringing problem). These are common inquiries received from customers, hopefully during the design phase, but, unfortunately, frequently during the evaluation stage. Each question deals with the response of a line receiver when normal data transmission breaks down, either intentionally, or from a system fault. Failsafe provisions provide a deterministic response to each of these conditions, ensuring that the receiver output goes to a "safe" condition when normal operation "fails".

Asynchronous systems have an inherent need for failsafe provisions. Suspended communications is typically signified by driving the line to a fixed state, with commencement of the next packet indicated by a "start" bit or "start" sequence. Receiving devices use the predefined transition sequence to detect the incoming data, and ignore the data circuit when the bus is not active.

Source synchronous clocked systems also need failsafe provisions integrated into their networks.
For example, consider a bussed communication system where a dynamic master sends out eight bits of parallel data, with a synchronous clock signal to latch in the data at each receiver node. After one node transfers its data, an idle time exists before a new master gains access to the medium, and begins communications. The status of the synchronous clocking signal is critical during this transition, as false transitions result in incorrect delivery of bytes to each receiving node.

A final example of a system needing failsafe provisions is a redundant, centralized, clock distribution system. In this case, two modules may be integrated to provide completely redundant synchronization signals. A primary clock source is designated, with a backup signal available when the primary clock is not present. Under failure conditions, such as a failed driver or shorted bus line, it is critical that each clock receiver detects the failure condition and transition over to the backup source. Incorporating failsafe mechanisms into each receiver contributes to robust failure detection, and responses.

**Previous solutions**

The most common approach to provide data line failure protection is via the use of external biasing components, an example that is shown in Figure 1.

**Figure 1: An external Failsafe bias network uses a resistor ladder to avoid ground faults.**

![Resistor ladder diagram](Click to Enlarge)

Resistors R1, R2 and R3 are chosen to match the characteristic impedance of the transmission medium, while also providing a bus bias voltage greater than the threshold for the receivers being used. Resistor R4 acts as a line-matching termination resistor, located at the far end of the transmission line. When choosing component values, R2 in parallel with (R1+R3) should equal the transmission media impedance, while R2 in parallel with R4 act as a voltage divider with R1 and R3 to set the failsafe bias voltage. The approach is desirable for the customization that is available for each unique application. The bias voltage can be set high enough to account for differential noise expected in the system, or low enough to take advantage of the known sensitivities of the receivers being used.

The drawbacks to this approach are that additional components must be included in the system and additional bias power must be used to energize the failsafe network. In the case where a failure condition includes receivers being disconnected from the communication bus, the external network provides no protection, as the receivers now have no access to the biased bus. Therefore, they will not achieve a fixed output unless other additional protection means are incorporated at each receiver. To simplify overall system design, minimize power and cost, and provide a more robust failsafe mechanism, many vendors providing LVDS devices have introduced integrated failsafe
receivers. The most common approach incorporates either internal pull-ups resistors to the VCC power rail or a pull-up resistor on one differential bus input pin and a pull down resistor on the complementary pin. The goal in either case is to establish a receiver condition leading to a predetermined output in the event that the input signal is lost.

There are pros-and-cons associated with some of these integrated approaches, as well as a unique integrated “active” failsafe protection implemented with a window comparator. Interchangeability is a common drawback of each of these approaches. Proprietary or customized designs often lead to systems where similar parts, from multiple vendors, behave differently to lost inputs. Whereas a designer may want to use a device thought to be available from multiple vendors, he might find himself depending on a single supplier due to non-standard behavior of the particular failsafe mechanism.

**Desirable characteristics of a failsafe mechanism**

With all the different failsafe protection methods available, designers may be uncertain which approach is optimum for a specific design. While there may be many good choices, the following features characterize a preferred approach. A preferred failsafe mechanism should provide open-circuit, short-circuit and idle-line detection and protection, over the full common-mode input range of the receiver. Providing protection under a limited set of operational conditions limits the robustness of the solution. A preferred approach should be integrated, requiring no additional bias components or power source, while also providing failsafe protection at each node, even under the condition where a node is removed from the network. Finally, and possibly most importantly, a failsafe mechanism should be standardized, allowing consistent performance and interchangeability when using components from different vendors.

**M-LVDS receivers**

The M-LVDS standard (TIA/EIA-899) is a general purpose multipoint specification that extends the benefits of LVDS to multi-driver designs. The standard identifies two classes of receivers, referred to as Type-1 and Type-2. Figure 2 shows the required response versus input differential voltage, for Type-1 and Type-2 devices. Type-1 receivers are similar to LVDS receivers, with thresholds centered on 0 Volts differential. Type-2 receivers provide a standardized failsafe approach by requiring an offset threshold. Bus input signals that are less than +50 mV are defined to be a low state, and signals greater than +150 mV result in a high state.

**Figure 2: Receiver differential input voltage threshold requirements.**

Type-2 receivers include the desirable failsafe features identified above. Under open-circuit conditions, the receiver input voltage approaches 0 Volts differential, and the output is forced low.
When the receiver input pins are shorted, similar behavior is observed. When all bus drivers are disabled again, the receiver differential voltage is limited to coupled differential noise, and the receiver output goes to a low state, and is guaranteed to stay low, unless the differential noise voltage exceeds the 50-mV threshold. Unlike some previous approaches, M-LVDS Type-2 receivers provide failsafe operation over a wide common-mode input voltage range. Failsafe behavior is ensured while the bus common-mode voltage varies from -1 V to 3.4 V, allowing Type-2 receivers to maintain failure condition protection even when the bus voltage is at the extremes anticipated by the M-LVDS standard.

The integrated approach provided by Type-2 receivers requires no external bias terminations or dedicated power supplies. When disconnected from the main bus, Type-2 receivers continue to "keep it safe." They do not rely on a remote bias network to charge the bus for those nodes that remain connected.

Type-2 receivers are standardized. Vendor A parts can be interchanged with Vendor B parts, without the concern of impacts on system software or compensating circuitry to force a common behavior. "Standardized" parts are truly standard compliant, rather than being nearly compatible.

**Noise margin concerns**

The experienced designer will realize that all these benefits must have some cost, and they do. Incorporating an offset threshold, either internally as in Type-2 receivers, or externally (by forcing a bias voltage onto the bus that must be overcome by the drivers), reduces the system noise margin. The noise margin is a supply-and-demand relationship. The drivers supply some minimum voltage, while receivers demand some maximum input voltage to guarantee operation. Figure 2 compared the thresholds for Type-1 and Type-2 receivers. Type-1 receivers only demand +/- 50mV, while a Type-2 receiver demands 150 mV before it is required to force the output high. There is clearly 100 mV less noise margin when using Type-2 devices than is available with Type-1 parts.

A more interesting noise margin comparison requires looking at LVDS (TIA/EIA-644A) receivers. LVDS receivers require +/-100 mV thresholds, implying that the loss in noise margin is now only 50 mV. This is further improved when using MLVDS drivers along with M-LVDS receivers. MLVDS drivers provide greater than three times the drive current of LVDS drivers, easily overshadowing the residual 50 mV noise margin cost of Type-2 receivers.

**Signal distortion concerns**

A final consideration that must be understood is signal distortion due to Type-2 offsets. Figure 3 provides a visual image of the potential distortion resulting from the offset in Type-2 parts. When thresholds are not centered on 0 V, symmetric inputs can result in asymmetric output patterns.

**Figure 3: Offset threshold impact on duty cycle: a higher offset raises the logic level**
Fifty percent duty cycle inputs can produce <50% duty cycle outputs, as the high time difference is less than 50% of the overall period (2*[t4-t1]). This distortion manifests itself as inter-symbol interference in random data streams or duty cycle distortion for clock signals. The level of distortion is dependent upon the edge rate of the input signal (t_{R}-t_{1}), as well as the offset value. When using offset receivers this effect must be considered and can limit the maximum useful signaling rate.

The M-LVDS family of parts from Texas Instruments (TI) support both Type-1 and Type-2 operation. The Type-2 receivers that TI offers have been designed with a duty cycle correction circuit that anticipates the potential duty cycle distortion, and pre-distorts the output signal to minimize the change in duty cycle. The resulting effect can be quantified by looking at some typical clocking frequencies.

**AdvancedTCA and M-LVDS**

Recognizing its benefits, PICMG has specified the use of M-LVDS as the electrical signaling standard for synchronization signals in AdvancedTCA systems. Synchronization signals up to 100 MHz are supported. A pair of standard clock frequencies can be examined to see the effectiveness of the duty cycle correction incorporated into the SN65MLV206, a Type-2, 100 MHz M-LVDS receiver. Table 1 compares the distortion introduced using Type-1 and Type-2 devices. The SN65MLV201 is used to demonstrate Type-1 receiver performance.

### Table 1: Duty cycle distortion due to offset threshold: Inputs and outputs should match for minimum distortion.
Clock frequencies of 19.44 MHz and 30.72 MHz have been used for comparison. 19.44 MHz is a SONET system clock signal, while 30.72 MHz is a WCDMA clock frequency. For each frequency, a high-slew rate input and a low-slew rate input were examined. The high-slew rate signal had a peak-to-peak voltage of 800 mV, similar to what could be expected from an M-LVDS driver over a short trace length. A high-slew full range transition time of 2-ns was used, again about what would be expected from an M-LVDS driver over a short trace length. The low-slew rate voltage swing was decreased to 400 mV, while the transition time was slowed to 4-ns, values that could be expected at the end of heavily loaded backplane system.

The results for the Type-1 receiver are not surprising. A 50% duty cycle input produced a 50% duty cycle output (within 0.5%). The SN65MLVD201 introduces little distortion. The bottom half of Table 1 highlights the benefits of the duty cycle compensation included in TI Type-2 receivers. The last column shows the expected duty cycle (assuming a 100 mV receiver offset, and accounting for the input signal characteristics). Higher slew rates minimize the effect of duty cycle distortion. The measured duty cycle column demonstrates that the duty cycle distortion, for the frequencies and test conditions tested, is less than 1%. Fifty percent duty cycle inputs will be very accurately recreated at the output of the SN65MLVD206, while still gaining the benefits of a standardized failsafe.

M-LVDS failsafe receivers provide a strong set of features that can be used to design robust systems that behave uniformly to fault conditions. These receivers can be integrated into designs using standard LVDS type drivers, where failsafe is needed, or into native M-LVDS systems, such as AdvancedTCA. The standardized approach available with M-LVDS allows more reliable use of devices from different vendors. With duty cycle compensation, as used in TI Type-2 receivers, the benefits of failsafe can be achieved without significant signal distortion. Deterministic outputs can be provided, with minimal impact to signal integrity. --