Converters for 3G are optimized for cost, size and power

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As communications systems have evolved from second-generation (2G) standards to third-generation (3G) standards, the performance requirements of the analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) used have also evolved. In original 2G basestations, designers often selected the highest-performance converters available to provide as much system margin as possible and improve manufacturability. This also allowed the manufacturer to differentiate its basestation with a performance advantage over its competitors—for example, a higher receive sensitivity.

Focus on cost
This is not usually the case with 3G designs, however. Industry demand for lower-cost systems and an ever-increasing array of features have caused designers to shift their priorities. Instead of focusing solely on performance, they are now focusing first on other system-enhancing elements, such as cost, power, size and integration, and secondarily on performance. This article will explore the transition from the highest-performance converters in 2G systems to the small, low-cost, low-power, highly integrated converters needed for 3G platforms.

As early 2G/2.5G systems were designed and deployed in the late '90s and early 2000s, many designers needed state-of-the-art converters to address the performance requirements for these systems. At that time, the highest available performance was found in the AD6645 14-bit, 80-MSPS pipelined ADC, which was designed on a bipolar process and consumed 1.5 watts. Similarly, the best-performing 14-bit, 100-MSPS DACs were based on bipolar or BiCMOS technologies and consumed more than 500 mW. Although this level of performance was required for early-generation systems, the devices represented leading-edge technology, so they tended to be somewhat costly.

As time has passed, the cost of the converter technology has decreased. Since that time, there are at least three 14-bit, 125-MSPS ADCs that dissipate less than 800 mW. With the introduction of these new competitive devices, the price of high-performance has decreased by at least 50 percent. Although these new devices do not equal the performance of the higher-power ADCs, they do offer extremely good performance at less than half the power of the first-generation device. The latest CMOS DACs, such as the AD9707, dissipate a mere 60 mW at 175 MSPS and outperform their BiCMOS cousins.

The first-generation ADCs were designed on a bipolar process, and the first-generation DACs were designed using 0.6-micron BiCMOS technologies. The current generation of converters is designed using 0.18-micron CMOS technology. This allows for much smaller die size, increased feature sets and lower power dissipation, all of which allow semiconductor manufacturers to support an overall lower cost structure. This benefit gets passed on to the end customer.

Power dissipation
At first glance, power dissipation would seem somewhat insignificant in a cellular basestation,
especially when considering that the power amplifiers (PAs) can output 40 watts. As basestation OEMs are looking to reduce cost, however, they are looking everywhere. In particular, some basestation deployments are now occurring at the top of towers directly connected to the PA itself. The advantage to this type of basestation is that it does not need to compensate for the cabling losses normally associated with putting the transceiver at the bottom of the cellular tower.

However, when a system is mounted at the top of the tower, no active cooling is possible, while the temperature must be kept as low as possible because there is a log-linear relationship between temperature and MTBF (mean time between failures). In addition to the cost of active cooling, OEMs are attempting to save money in the mechanicals of the basestation. Higher-power converters without active cooling require the mechanical unit in which the transceiver is housed to be more complex and more expensive in order to dissipate the heat efficiently.

Converter manufacturers have addressed power concerns through advances in process technology and architectural changes. As mentioned previously, the latest ADCs and DACs are being designed in fine-line CMOS technologies. This greatly reduces switching transients in the logic cells. In some cases, dynamic logic elements are employed, further reducing switching transients by using a parasitic capacitance to store the logic state. In the case of ADCs, the architecture has transitioned from pure flash to pipelined single-bit and multibit converters, greatly reducing the number of comparators required and hence the overall power. The data in Figure 1 demonstrates the dramatic decrease in power consumption for 12-bit and 14-bit ADCs during the last decade.

![Click to Enlarge Image](image)

**Figure 1: Flyback Converter Design**

### Size

Like power dissipation, size has become a major factor in determining the best converter for an application. In deployments such as the tower-mounted system mentioned above, OEMs are not only limited on power, but are also trying to implement more carriers on the same form factor that originally supported a single sector of a basestation. This increased density allows operators to deploy more carriers and thus support more users in heavily populated areas.

In addition to simply reducing the actual size of the converters, another trend is increasing integration. Digital-to-analog converters now include extensive digital signal processing, such as interpolating filters, complex modulation, inverse sinc filters and numerically controlled oscillators (NCOs). For ADCs, integration has included adding NCOs and decimating filters to improve performance. Both interpolating filters for DACs and decimating filters for ADCs have the added benefit of reducing the high-speed switching noise between the converter and the digital logic.

While it may not be obvious, new-generation converters have also reduced size by enabling simpler architectures. In particular, new low-power, high-performance DACs now make direct-conversion
architectures feasible. In early generations, a low intermediate frequency (IF) was used, and then multiple mixer stages were used to achieve the proper RF signal, Figure 2a.

By removing multiple mixers and amplifiers from this signal chain, as shown in Figure 2b, a significant size and cost advantage can be realized.

Although direct conversion has not yet been realized for basestation receivers, the IF-sampling capability of many A/D converters has been greatly improved. It is now possible to IF sample at up to 450 MHz and maintain very good performance. That will allow the removal of a single mixer stage and again reduce overall system cost.

Performance Although performance is still an important factor, it is no longer the first priority for most designers. As the number of competitors in the converter space has increased over the last five to seven years, the number of basestation suppliers has also increased. This, in conjunction with the high price paid by operators for 3G licenses, has led to increased cost pressure for all basestation OEMs.

It is this cost pressure that has forced many designers to look at converters that just meet the system requirements instead of paying the price premium for the highest performance converters. The good news for many designers, though, is that it is easier to meet many of the 3G (W-CDMA) converter requirements for the 2,100-MHz band than those of the GSM 900-MHz band. For example, a 12-bit, 65-MSPS ADC and 14-bit, 65-MSPS DAC can meet the requirements for a two-carrier W-CDMA system, and a 14-bit, 65-MSPS ADC and 14-bit, 125-MSPS DAC can meet the requirements of a three- to four-carrier system.
On the other hand, only a small number of ADCs and DACs can meet the requirements for the multicarrier GSM 900-MHz band. These, as noted, represent leading-edge technology and thus carry a price premium. Multicarrier and multistandard architectures utilizing leading-edge converters can lower overall development and manufacturing costs by reducing the number of design variants required, but that must be weighed against the higher bill-of-materials cost.

**Conclusion**
It's clear that the driving force behind choosing a converter for a basestation design is to remove cost from the system. Cost is manifested in many subtle ways, including power dissipation, size and performance. These attributes affect choices such as system architectures, number of carriers and even deployment locations. This shift in thinking is driving many converter manufacturers to introduce parts that meet as many of these dimensions as possible. Since it's very difficult to meet every attribute with a single device, a broad product portfolio offers the best chance of providing the right converter for the specific radio architecture and performance requirements.

**About the author**
Chris Cloninger joined Analog Devices Inc., [www.analog.com](http://www.analog.com) in 1995 after receiving a bachelor's degree in computer engineering from Clemson University. He is a mixed-signal marketing/systems engineer for high-speed analog/digital converters for wireless infrastructure and can be reached at chris.cloninger@analog.com.