Understanding Continuous-Time Sigma-Delta ADCs

Scott Kulchycki, Staff Engineer, Data Conversion Division, National Semiconductor Corporation - May 27, 2008

Continuous-time sigma-delta (CTΣΔ) analog-to-digital (A/D) conversion technology is challenging the conventional wisdom that pipeline A/D conversion is the only technique available for high dynamic performance, sub-100 MSPS (megasamples per second) applications. This article first reviews data conversion fundamentals and then provides a comparison of pipeline A/D converters (ADCs) and ΣΔ ADCs, along with a brief overview of the industry's first 12-bit, 50-MSPS ΣΔ ADC. The article concludes with a summary of the features that make it easy to deploy ΣΔ ADCs in high-speed, high performance systems.

Data conversion fundamentals
ADCs perform two basic, fundamental operations: discretization in time and discretization in amplitude. The two functions are shown conceptually in Figure 1, though the actual ADC may not be structured as such.

![Figure 1: Analog-to-digital conversion](Click to enlarge image)

The first operation of the ADC is to discretize in time, or sample, the continually time-varying input analog signal, x(t). The input signal is typically sampled at uniformly spaced times at a frequency of f_s, and the samples are thus separated by a period T = 1/f_s.

Once the input signal is sampled, the resultant exists only as impulses at the sampling interval, kT. However, this sampled signal is still able to assume an infinite range of values, and therefore cannot be represented precisely in a digital form.
The second function of the ADC is to discretize the sampled signal in amplitude. That is, the ADC approximates the amplitude of each sample with one of a finite number of possible values. Because the output of the ADC can take on only a finite number of possible values, the amplitude of each sample can be represented by a digital code whose bit length determines the total number of possible converter outputs. The finite number of output values in a converter introduces error into the digital representation of the analog input. This so-called quantization error limits the resolution of the converter.

**ADC Architectures**

In general, ADCs are divided into two broad categories: Nyquist-rate converters and over-sampling converters. These different converter classes typically offer different compromises between ADC resolution and output sampling rate.

**Nyquist-rate converters**

Nyquist-rate converters are those that operate at the minimum sampling frequency necessary to capture all the information about the entire input bandwidth, and therefore the output data rate of a Nyquist-rate converter can be very high. Three of the most popular Nyquist-rate converter architectures are SAR (successive approximation register), flash, and pipeline ADCs. This article focuses on the differences between pipeline ADCs and ΣΔ ADCs, which are very different from discrete-time (DT) ΣΔ ADCs.

**Pipeline ADCs**

Pipeline ADCs have become the standard in data conversion applications at 8-bit and higher resolutions for sampling rates from 5 MSPS to 200 MSPS or more.

Rather than providing enough comparators to check the input against every possible input value as in a flash ADC, the pipeline architecture employs multiple, low-resolution flash-conversion stages cascaded in series to form the pipeline. Each stage in the pipeline quantizes its input, then sends the error in that quantized estimate on to the next stage for further quantization (Reference 1) This process is repeated several times as the signal progresses through the pipeline until the LSBs are determined and the output of all the stages in the pipeline are then combined to form the overall digital approximation to the input sample value.

Because the pipeline is able to operate concurrently on many samples, the ADC outputs a complete digital word every clock cycle. This parallel processing allows the pipeline to offer high resolution at the full Nyquist rate of the converter. But the tradeoff for the high output rate is a delay from when the input is first sampled to when its digital approximation is made available. This delay is known as the latency of the pipe, which is typically on the order of ten sample clock cycles. Fortunately for many applications, the latency of a pipeline ADC is acceptable.

**Challenges of the Pipeline ADC**

Pipeline ADCs are capable of providing high dynamic performance at sampling rates up to 100s of MSPS. Although the pipeline architecture can achieve very high frequency operation at moderate-t-high resolution, it compromises in other design parameters.

**High-Speed Circuits**

Because each stage in the pipeline must process the previous stage's output, a constant input during the conversion process usually is provided in each stage by a sample-and-hold (SHA) circuit (Reference 1). The first-stage SHA must maintain the accuracy of the overall ADC at the full sampling rate, requiring the switched-capacitor circuit to settle within a single clock period (Reference 2). Similarly, the first-stage adder and DAC must be able to settle their outputs within a single period. These speed requirements for the first stage (and to a lesser extent for subsequent
stages) typically require large-bandwidth amplifiers and other circuits, which can lead to high power consumption.

**Thermal Noise**
The maximum dynamic range of the pipeline ADC is determined at least partly by the thermal noise at the input of the converter, including the kT/C noise of the input sampling capacitor. To reduce kT/C noise, a larger capacitor can be used, but at the cost of increased switching noise at the input and a more difficult-to-drive input, requiring a higher-performance, higher-power ADC driver.

**Migration to Future CMOS Processes**
As for all sampled-input ADCs, pipeline ADCs are also challenging to migrate to future CMOS processes. This challenge arises from the switched-capacitor input, as a boosted CMOS switch is often used to sample the input signal onto the sampling capacitor. As CMOS processes and their supply voltages shrink, the overdrive voltage available for the CMOS switches also shrinks, greatly reducing the range of input voltages that can be sampled with high resolution. Furthermore, designing switches with reduced threshold voltages that work well in deep sub-micron processes can be difficult.

**Input Filtering and Sampling Clock Requirements**
A final challenge in using any sampled-input ADC, including pipelines, concerns the external circuitry necessary to drive the converter (Reference 2), specifically the input-filtering network and the sampling clock. With any sampled-input converter, signals that can be aliased into the band of interest by the sampling operation must be eliminated using an anti-aliasing filter (AAF).

Steep attenuation characteristics are hard to achieve in an external analog filter, leading designers to over-sample the signal of interest. Although over-sampling reduces the range of frequencies that can alias down in-band and hence, lowers demands on the AAF roll-off, over-sampling the ADC wastes the Nyquist bandwidth, which increases system power. In addition, over-sampling increases the processing demands on subsequent digital circuitry.

The sampling clock provided to the ADC is another important determinant of the overall dynamic performance of a sampled-input ADC, especially for high-resolution, high-input frequency applications (Reference 2). The phase noise of a clock source will appear as increased noise at the ADC output and therefore, care must be taken by the system designer to ensure the overall system resolution is not limited by their clock source. Clock quality is especially important for high-speed, high-resolution ADCs because the demands on the purity of the clock increase with increasing input frequency and increasing ADC resolution.

It is apparent from the preceding discussion that, although they are excellent candidates for high-speed, high-performance applications, pipeline ADCs do present design challenges for both the ADC designer and the system designer using the ADC. In contrast, CTΣΔ ADCs do not require fast-settling circuits or switched capacitors at their inputs and thus avoid the increased ADC power and need for high-performance drivers in high-resolution applications. CTΣΔ ADCs also include significant anti-aliasing filtering, reducing or eliminating the need for an external AAF and preventing wasted ADC bandwidth. Finally, CTΣΔ technology is well-suited for migration to future CMOS processes.

**Continuous-Time ΣΔ Modulators**
The first recognizable CTΣΔ modulator, introduced in 1962, was actually implemented as a CT circuit (Reference 3). Indeed, CT implementations of ΣΔ modulators have appeared regularly since then, but when switched-capacitor (SC) circuits were introduced, most CTΣΔ modulators were implemented with DT loop filters. SC circuits remain popular because of their insensitivity to signal waveform characteristics.
In addition, the time constants of SC integrators scale with sampling frequency, allowing for greater system flexibility (Reference 4). However, interest in CTΣΔ modulators has been renewed because of their benefits versus sampled-input ADCs, such as employing lower-power integrator amplifiers and including inherent anti-aliasing filtering (Reference 3).

CTΣΔ ADCs differ from sampled-input ADCs, such as pipeline and DTΣΔ ADCs, in two important ways:

- A CTΣΔ modulator uses CT integrators rather than DT integrators or circuits. That is, rather than SC circuits, a CTΣΔ modulator employs continuous-time circuits, often RC or C/gm integrators.
- The sampling operation in a CTΣΔ modulator occurs at the output of the forward loop filter, before the quantizer. In contrast, for a sampled-input ADC, the sampling occurs at the input of the ADC.

These differences between CTΣΔ ADCs and pipeline ADCs give rise to significant performance differentiation between the two. Specifically, CTΣΔ ADCs operate at lower power, include significant anti-aliasing filtering (Figure 2), and present a much quieter input stage.

![Figure 2: Anti-aliasing performance of ΣΔ and pipeline ADCs.](Click to enlarge image)

### Challenges of the ΣΔ ADC

Of course, as pipeline ADCs offer high-speed operation while compromising other design parameters, the benefits of CTΣΔ operation also come at the cost of some design challenges for both the ADC designer and the system architect. A sampled-input, SC ADC can often operate over a wide range of sampling frequencies from near-zero to its maximum rate. However, the dynamics of the CTΣΔ are set by the RC or C/gm product of its component integrators; therefore, the integrator time constants must be tunable to allow for process variation (Reference 2). In addition, the loop dynamics will not scale with sampling frequency, limiting the allowable sampling-rate operating range.

The input bandwidth of a ΣΔ is also limited to the ADC's first Nyquist band. In a Nyquist-rate ADC wherein full-rate sampling occurs at the system input, the input bandwidth can be many times larger than the Nyquist rate of the converter, allowing for IF-sampling. Conversely in a ΣΔ ADC, because of the lowpass decimation filtering, signals outside the first Nyquist zone will be removed from the output spectrum. In addition, although a DTΣΔ would allow signals around its loop sampling rate, \( M_f \), where \( M \) is the modulator over-sampling ratio, to fold down inband, the inherent anti-aliasing filtering in a ΣΔ ADC precludes this from happening. Therefore, input signals must be mixed down into the first Nyquist zone to be digitized by a ΣΔ ADC.

Finally, because of its over-sampling operation, the output rates of ΣΔ ADCs are currently limited to
less than 100 MSPS while pipeline ADCs are capable of operation up to 500 MSPS and beyond. Indeed, for a given technology, Nyquist-rate converters will always be able to operate faster than ΣΔ ADCs because of the over-sampling necessary in a ΣΔ design.

Fortunately, the benefits of CΣΔ technology outweigh the drawbacks for high-resolution applications at sampling rates below 100 MSPS.

**Industry's First ΣΔ ADC**

ΣΔ A/D conversion technology has proven that pipeline ADCs are not the only conversion technique available for high dynamic performance, sub-100 MSPS applications. The benefits of CΣΔ technology are now available in National's recently introduced ADC12EU050, a 12-bit, ultra-low-power octal ΣΔ ADC with an alias-free sample bandwidth of 20 MHz to 25 MHz and a conversion rate of 40 MSPS to 50 MSPS (Figure 3).

The ΣΔ technology on which the ADC12EU050 is based includes inherent anti-aliasing filtering and provides a low-noise, easy-to-drive input stage. To fully exploit these considerable benefits of CΣΔ technology, the ADC12EU050 also includes an on-chip clock conditioner that eliminates the need for an expensive high-performance clock. Finally, the ADC12EU050 avoids the hazards of input overload present in ADCs by offering a means for recovering immediately from an input overload event.

**Summary**

Besides providing more power-efficient operation, ΣΔ technology also offers unique features that greatly reduce the challenges of deploying such ADCs in high-speed, high-performance systems. In short, ΣΔ technology offers:

- An inherently power-efficient architecture that eliminates the high-speed gain stages required for sampled-input ADCs, such as pipeline or traditional DTΣΔ ADCs.
- An essentially alias-free Nyquist band that is made available by exploiting inherent over-sampling, an internal lowpass CT loop filter, and on-chip digital filtering.
- A purely resistive input with no switching, which is easier to drive and couples less noise to the overall system than the switching input capacitors of a sampled-input ADC, such as a pipeline or DTΣΔ ADC.
• An on-chip clock conditioning circuit to provide the over-sampling clock to the internal modulator. This circuit increases the frequency and the quality of the input clock, yielding a low-jitter sampling edge and achieving high-resolution performance without an expensive, high-performance input clock.

• Easier migration to future CMOS process technologies. In a ΣΔ ADC, the impact of noise and nonlinearity associated with the sampling process is significantly reduced, allowing for the reduced supply voltages required for future CMOS processes.

Taken together, the inherent benefits of ΣΔ technology and the opportunity to implement an on-chip clock conditioner greatly simplify the signal path design by:

• Reducing power requirements.
• Eliminating the need (or reducing the requirements) for an external anti-aliasing filter.
• Reducing the input-driver requirements.
• Mitigating the need for high-quality clock sources without sacrificing performance.

Additionally, the ability of ΣΔ ADCs to scale with technology will allow such designs to take full advantage of future CMOS processes.

References

About the Author
Scott D. Kulchycki is a Staff Engineer in the High-Speed Data Conversion Products Group at National Semiconductor Corporation, Santa Clara, California. He received his Ph.D. in electrical engineering from Stanford University; his doctoral work focused on continuous-time sigma-delta ADCs.