What to consider when using self-protected MOSFETs in ruggedized electronic systems

Don Zaremba, Applications Manager, ON Semiconductor - February 12, 2006

Power devices used in automotive electronic systems must endure extremely harsh environmental conditions. Devices must withstand high voltage spikes resultant from switch-off transients and load dump faults. Ambient operating temperatures exceeding 120°C push device junction temperatures higher. The numerous connectors in wiring harnesses, in place for ease of assembly and repair, afford opportunity for intermittent electrical connection to devices. Even normal operating conditions can significantly stress devices as new loads require ever increasing power.

In order to improve system reliability and reduce warranty costs, designers incorporate fault protection circuitry with power devices, to prevent device failure and subsequent costly damage to the electronic system. Often this is accomplished via external sensors, discrete circuitry, and software, but more commonly designers utilize fully self-protected MOSFET power devices. As technology advances, these devices offer superior fault protection at lower system cost.

Figure 1 shows the general topology of a fully self-protected MOSFET. Other features commonly found on these devices include status indication, digital input, differential input, and over-voltage and under-voltage lockout. High side configurations include on-chip charge pump capability. However, the three circuit blocks common to most devices that provide most of the device protection are current limit, temperature limit, and drain to source over-voltage clamping.

![Figure 1 Self-protected MOSFET topology](image)

**Common faults**

Perhaps the most common and worrisome fault is a short circuit. This type of fault can take several forms: a short across the load, a short across the switch, or a short from supply to ground. Moreover, these shorts occur when the device is both on and off. Such conditions are further...
exacerbated since short circuit faults are often intermittent and take many forms during even very brief periods. For example, in the case of a short across the device with the MOSFET off, current is diverted around the MOSFET thru the short. However, if the short is intermittent and the load is inductive, the interruption of the current flow results in a flyback voltage appearing across the MOSFET. The peak current in the load inductance could be higher than normal operation due to the duration and resistance of the short circuit. Thus the device may absorb more energy than expected, and numerous intermittent short events occurring in quick succession could result in elevated peak junction temperature, leading to potential device destruction.

Other faults include electrostatic discharge (ESD) at the device pins, over-voltage due to line transients or inductive load switching, and over heating. Over temperature failure typically results from another failure such as short circuit which vastly increases device power dissipation, but also results from extreme ambient conditions or thermal path anomalies such as a solder void between the device heat-sink and circuit board. The control circuitry of self-protected MOSFET products detect and control device operation during many of these failure modes by operating in a safe mode so the device can return to normal function once the fault is remedied.

Since active components other than the MOSFET gate oxide interface are connected to the gate input pin, the current leakage at this pin with the drain shorted to the source can be three orders of magnitude greater than the same leakage measurement on standard MOSFET (50-100µA versus <50na). This increase in leakage current usually does not pose an issue for gate drive circuitry; however, if the gate drive circuit is capable of driving enough current during an a current limit or thermal shutdown fault condition during an over-current and over-temperature fault conditions, the device normally pulls the power mosfet gate node voltage down to near threshold voltage for saturation operation or to zero volts to turn the device completely off. Usually a series resistance (rs) exists between the gate input pin and the power mosfet gate node, so input current draw is approximately equal to (vin-gate)/rs. Usually devices are designed to turn off when the junction temperature exceeds a pre-set limit. In this case, if the gate voltage is zero volts, so is the minimum source current to obtainvin/rs must be available during an over-temperature fault. If not, the internal gate pull-down circuit may not keep the device power off, possibly allowing the junction temperature of the power fet to reach destructive level.

Over-temperature protection usually is established by biasing temperature sensitive devices (normally diodes) located in the active area of the main power MOSFET. If these elements detect a die junction temperature greater than the over-temperature set-point, a circuit pulls the main power MOSFET gate to ground, turning off the device. Some devices incorporate a hysteresis circuit allowing the device to turn back on after the die junction temperature cools by some small delta, on the order of 10°C - 20°C. This is demonstrated in Figure 2 which shows the short circuit current versus time response for an ON Semiconductor NIF5022N device. In other devices, the current latches off when an over-temperature fault condition is detected, and the input pin must be toggled to reset the latch.
Over-temperature conditions

Two main issues must be considered during over-temp fault conditions. First, the temperature limit shutdown circuitry usually works in concert with current limit circuitry. That is, the current limit circuitry drives the device into a saturation operation mode by driving the gate node to near threshold voltage in order to maintain a current limit set-point. In the case of a short circuit across the load, this means the voltage drop across the power MOSFET approaches the supply voltage while passing high current. This high power situation quickly leads to an over-temperature fault condition. For devices that utilize thermal hysteresis to cycle the part on and off during an over-temperature fault condition, the junction temperature will stabilize to a temperature somewhere between the high and low set-points of the hysteresis circuit. This is akin to a high temperature reliability test, depending on the length of time the device operates in the fault condition. Normally one does not expect to operate the device in a fault condition for thousands of hours or more, when degradation of device reliability may become of valid concern. Of more practical concern is when the application circuit cycles the gate input pin on and off during a fault condition, allowing time for the junction temperature to cool between over-temperature events. In this case, the device under goes internal thermal cycling, and the number of thermal cycles the device withstands may have a finite limit. How many cycles depends on many factors including the delta junction temperature magnitude, temperature sense layout and circuit design, silicon construction, packaging technology, and others. A designer must establish if the application circuit can cycle the protected MOSFET during a short circuit or other fault condition that invokes over-temperature protection and then evaluate device reliability under these conditions. Such failure mode analysis may eliminate costly field returns.

The second issue concerns device operation where the over-temperature protection is not active and subsequent device failure is possible. When switching off an inductive load, the device must absorb the energy stored in the load inductor. For standard MOSFETs, this operation mode is known as Unclamped Inductive Switching (UIS). During a UIS event, the device drain to source silicon junction is in avalanche and significant power is dissipated by the device, dependent on the avalanche voltage and peak current value. The normal failure mode for an UIS event occurs when the energy absorbed by the MOSFET raises the junction temperature above the intrinsic temperature of the silicon structure, typically greater than 300°C. When the junction temperature exceeds the intrinsic temperature, the device stops behaving like a semiconductor, gate control is lost, and device destruction quickly occurs unless drain supply power is immediately removed. Self-protected MOSFETs can suffer this same fate, since in cases where the control circuitry is biased by the gate input voltage, the over-temperature limit circuit is inactive since gate bias is zero. The circuit designer must ensure during normal operation and worst case fault conditions (such as the case of intermittent short across the device) the energy absorbed by the device does not exceed maximum ratings. In addition, even if the maximum energy rating is observed, sufficient time between energy pulses must be allowed so that the junction temperature can cool down back to the initial starting junction temperature. Otherwise, the junction temperature ratchets up after each energy pulse, eventually reaching the intrinsic failure temperature.

In the case where over-temperature limit circuitry is biased during inductive load switch-off, over-temperature protection may still not be active because most self-protected MOSFETs utilize active over-voltage clamping. The key component in the active clamp circuit is the back to back zener diode.
string located between the main power MOSFET gate and drain connections. The zener voltage of this stack is designed to be less than the avalanche voltage of the main power MOSFET drain to source junction. When the drain voltage rises above the gate to drain zener stack voltage, current will flow through the stack and thru a series gate resistance to ground, since the gate is switched off. Thus a voltage near threshold at the main power MOSFET gate is developed allowing the MOSFET to conduct load current in a forward, linear operation mode. The inductive energy is dissipated with a more uniform current density in the active region, since the device is turned on, as compared to dissipating the energy in an avalanche operation mode. Moreover, since the clamp voltage is lower than the avalanche voltage, the device dissipates less instantaneous power in an active clamp mode than in an avalanche mode. These behaviors afford the device greater energy handling capability when switching inductive loads in active clamp operation mode. Because of this feature, active clamp operation often takes precedence over other fault protection operation. The designer must ensure the device is capable of absorbing all conceivable inductive energy under worst case conditions.

In summary, utilizing self-protected MOSFETs can yield a cost-effective fault tolerant system design. However operating conditions do exist that can damage or destroy self-protected MOSFET devices. Careful consideration of these factors during system design will result in cost effective, reliable system.

Author info
Don Zaremba is Applications Manager for ON Semiconductor’s Integrated Products Group – focused on power MOSFETS, smart MOSFETs, and ignition IGBTS. With more than 20 years of industry experience at ON Semiconductor and Motorola, he has held both applications engineering and wafer manufacturing management positions. Zaremba earned his BSEE from UCLA and has completed Advanced Applied Statistics studies at ASU. Email: d.zaremba@onsemi.com; Tel: 602/244-4785