How to detect solder joint faults in operating FPGAs in real time

Phillip Davies, Ridgetop Group - March 04, 2009

The problem: Solder joint faults in FPGAs
Solder joint faults can be described with a single word – pernicious. Solder joints connect the BGA package, containing an FPGA (Field Programmable Gate Array) core, to the PCB (Printed Circuit Board). Without early detection, electrical anomalies caused by solder joint faults can result in the catastrophic failure of mission-critical equipment.

In order to prevent this, Ridgetop Group designed the Sentinel SJ BIST EPU (Solder Joint Built-In Self-Test Electronic Prognostic Unit). Part of a line of electronic prognostic solutions, SJ BIST provides real-time detection of solder joint faults in any operating FPGA for military, aerospace, and automotive applications.

Solder joint faults can occur with FPGAs found in all types of commercial and defense products. When embedded in BGA (ball grid array) packages, FPGAs become susceptible to failure from solder joint faults. The causes of solder joint faults cannot be isolated, early detection is difficult, and the intermittent failures escalate in severity until devices are rendered unreliable or inoperable. But, as so often seems to be the case, the problem is also the solution...

Stress-related faults
In operational devices, the primary contributors to solder joint faults are thermo-mechanical and shock stresses. Whether from vibration, torque forces, thermal cycling, material expansion, or environmental stresses, the inevitable result is mechanical failure from cumulative damage. At the solder joint level, the damage is seen as a crack at the package/PCB boundary, although there are other possible points of failure in the solder joint network.

Statistical degradation modeling is the current method for predicting solder joint faults in programmed, operating FPGAs. However, since statistics vary and work best at trending large populations, statistical degradation modeling is a stop-gap solution, at best. With SJ BIST, Ridgetop Group provides a true tool for direct, in-situ measurement of prognostic indicators of faults in operating solder joint networks.

Manufacturing-related faults
Since solder joint faults develop during manufacturing as well as in the field, SJ BIST can also be used to detect faults in uninstalled FPGAs. These manufacturing-related faults have their own set of detection challenges. Visual inspection is the current method used for identifying faults in the manufacturing environment. The primary disadvantage is the inability to test and inspect the solder joints.

Visual inspection is limited to the outer row while the board size and other surface-mounted components limit the view even further. As the array density of BGA packages increases, alignment
tolerances become tighter. In fine pitch BGAs, there are thousands of solder balls with a 1.0 mm pitch and a 0.60 mm ball diameter. Under these conditions, pad misalignment and insufficient solder become causes of open and partial-open faults.

Even a 100% inspection by X-ray is not guaranteed to find solder joint faults when solder does not wet the entire pad. Another defect, involving the solder ball and paste wicking into a plated through hole, is not readily identifiable even with X-ray imaging. When enough solder wicks into a hole, an open fault is created for that lead.

As an in-situ softcore, SJ BIST is ideally suited for PCB-FPGA reliability testing in manufacturing for harsh environments.

**Failure definition**

An industry standard defining BGA package failure involving thermal cycles, with or without accompanying physical stresses, is the occurrence of:

1. A high-resistance spike of 300 ohms or higher for a duration period of 200 nanoseconds or longer.

2. Ten or more events that occur within 10% of the time (number of thermal cycles) of the first event.

**Types of solder joint failures**

**Solder Ball Cracks**

Over time, solder joints can develop cracks from cumulative stress damage. Cracks typically appear in the package/PCB boundary. A crack can cause the partial separation of the solder ball from either the BGA package or the PCB.

One typical location for a crack is between the BGA package and the solder ball. Another typical location for a crack is between the PCB and the solder ball. Progressive damage to a cracked solder ball leads to another type of failure – the fracture.

**Solder Ball Fractures**

Once a crack develops, progressive stresses can cause more damage leading to a fracture. A fracture is the complete separation of a solder ball that breaks that point of contact between a BGA and PCB.

As existing fractures remain open for longer periods, contamination or oxidation coats the fracture surfaces. This eventually creates a failure progression from degraded joints to intermittent opens of short duration (nanoseconds) and then relatively long durations (microseconds).

**Missing Solder Balls**

The progressive mechanical stresses that lead a crack to form a fracture end in displacement. A displaced solder ball not only results in a permanent failure for that pin, the highly conductive ball could be lodged in another location and cause an unwanted short in another circuit.
Intermittent Signals

Intermittent signals are caused by solder ball fractures that periodically open and shut. Vibration, motion, thermal, and other stresses cause conditions where a solder ball can move enough to open or shut a fracture. The flexible materials used in PCB fabrication make intermittent signal failures possible. As vibration stress, for example, causes a fracture to open and shut, the circuit of that solder ball unpredictably opens and closes, resulting in an intermittent signal.

The intermittent nature of solder joint failures makes faults hard to diagnose. Also, the input and output buffer circuitry of an I/O port makes it impossible to measure the resistance of a solder point network belonging to a programmed, operational FPGA. Often, a bench-tested assembly passes as No Trouble Found (NTF) because damaged joints make temporary contact.

Solder Joint No Fault and Fault Tests

The two signal traces illustrated in Fig 3 are for voltages on a 1.0 µF capacitor connected to a group of two I/O ports. The first trace (A) shows the capacitor voltage when one of the two ports connected to the capacitor has a 1 ohm resistor connected in series with the solder joint: the resistance is not high enough to cause a write fault to occur, and SJ BIST correctly did not report a detected fault.
The second trace (B) shows the occurrence of a write fault when the capacitor voltage resistance is increased to 100 ohms.

3. SJ BIST: 1 MHz Capacitor Signal. Top (A) is for a No Fault Condition (1 ohm); Bottom (B) is for a Fault Condition (100 ohms) [0.5 µs × 2.0V grid].

For clock frequencies of one-half or higher of the maximum clock frequency of the FPGA, the capacitance of the I/O port is sufficient such that no external capacitance needs to be connected, and SJ BIST correctly detected faults with zero false alarms.

Recent analysis of the test data produced and collected by Ridgetop's test lab, as well as the Center for Advanced Vehicle Electronics (CAVE) in Auburn, AL, a major automotive manufacturer's test lab, plus research literature, demonstrate with a 95% confidence level that the first BGA pins to fail are at or near the corners of an FPGA package. The solution: SJ BIST

Prior to Ridgetop Group's innovation, there were no known methods for detecting stress faults in operational, fully-programmed FPGAs. The visual inspection, x-ray imaging, and reliability tests used in manufacturing are ineffective because electrically-based defects are essentially invisible in powered-down devices.

Through early detection of impending faults, SJ BIST supports condition-based maintenance and reduces intermittent failures. Its outstanding sensitivity and accuracy allows the SJ BIST to detect and report high-resistance faults as low as 100 ohms as fast as a one-quarter to two clock cycles with no false alarms. Developed as a large-scale solution, it attaches to the customer's existing, built-in, test backbone. Due to its scalability, there is no point of diminishing returns.

Ridgetop Group's SJ BIST is a licensable IP core, part of the InstaBIST library, and requires no tools or equipment to install. As a Verilog softcore synthesized into a customer's FPGA, SJ BIST is minimized for the thrifty designer. Conscious of ever-shrinking real estate, the only additions are
small capacitors to the PCB and a small code base to the existing test program. Under certain conditions, the capacitors may not be required.

**The solution is the problem**

So just how does SJ BIST work? As mentioned before, the problem is the solution. The same electrical changes in solder joints causing faults can be exploited to indicate accumulating damage and to prognosis failure conditions well before catastrophic failure. The shortcoming of previous detection methods is their indirect approach to assessing what is happening electrically. Visual inspection, x-ray imaging, and failure analysis modeling are indirect, imprecise, and non-specific at the individual fault level.

In contrast, SJ BIST directly and in real-time measures and records the electrical properties of dedicated, operational pins and solder joints. This method detects and recognizes signal characteristics or changes indicating damage prior to catastrophic failure. To put this concept another way, SJ BIST is analogous to an EKG.

**A Real-World Analogy - the EKG**

The EKG (electrocardiogram) measures and records the electrical activity of the heart. Abnormalities in the cardiac signal are seen in real-time and, naturally, while the heart is in operation. While this alone is a great advantage over reliance on indirect measurements, such as blood pressure, the EKG has an even greater ability: prognosis. Libraries of cardiac signals document the early electrical characteristics of heart conditions.

This means that before a heart condition can be felt via performance degradation, changes in electrical activity are detected, analyzed, and correlated against a library of signal abnormalities to provide a prognostic determination. This technique, when applied in medical science, has led to the advance warning of many serious, even life-threatening conditions, and extended life expectancy.

**SJ BIST - In Your World, In Your Business**

Just as use of the EKG can extend people's lives, the benefits of SJ BIST for extending the operational life of electronic devices is impressive. The InstaBIST library developed by Ridgetop Group makes solder joint fault prognosis possible. Through direct analysis of the real-time electrical activity occurring in FPGAs, SJ BIST detects the faults and the indicators of progressive fault conditions.

SJ BIST is an ideal solution for the automotive, industrial, and aerospace markets. Medical electronic devices are also a natural fit. Pacemakers, neurostimulators, and other devices placed directly in or near the heart, brain, and spinal cord require high reliability. Electronic prognostics from Ridgetop Group would enable safe removal and replacement before problems could develop.

IP licenses for SJ BIST start at $50K and include technical services for installation. Training, documentation, service contracts, and other technical services are available.

**About Ridgetop**

Ridgetop Group ([www.RidgetopGroup.com](http://www.RidgetopGroup.com)) is a privately held firm founded in 2000 to provide mission-critical electronic prognostic tools, fault-to-failure progression libraries, and semiconductor IP libraries through excellence in engineering innovation.

Phillip J. Davies oversees Ridgetop’s Sales and Marketing functions. He has extensive sales and marketing management background with over 30 years of business development experience in delivering technology solutions for commercial and aerospace customers. Phil has established effective sales, marketing, product definition, program management, and customer service teams worldwide for large corporations and small entrepreneurial companies.

Previously, Phil held positions as Division Manager at Sigma Data Systems, a software development company, and Director of Sales and Marketing at both Gain Technology, (acquired by SMSC), and AlliedSignal (Honeywell). At these companies, he managed all business development functions including business strategy and channel sales worldwide to drive growth in software intellectual property licensing, design services, and manufacturing services. Phil holds a BS degree in Engineering from San Jose State University, and an MBA from Regis University. Phil can be contacted at Phil.Davies@RidgetopGroup.com.