How to reduce power consumption in CPLD designs with power supply cycling

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It is increasingly common for Complex Programmable Logic Devices (CPLDs) to be used in systems with stringent power budgets. Examples include smart phones, handheld instrumentation, video recording equipment, and navigation devices. Although a number of "zero power" CPLDs exist with standby power measured in microamps, these devices often don't have the features required for a particular design. In these cases, power supply cycling offers designers a viable means to achieve the desired features as well as low power consumption.

The duty cycle approach to power consumption reduction relies on the fact that for much of the time equipment is operational there is often little processing required by the CPLD. For example, the CPLD may be scanning a key pad to see if a key press has occurred, or is waiting for some communication on a serial interface.

CPLDs, like all integrated circuits, consume some power associated with device bias and leakage, regardless of activity. This power is often referred to as static current. CPLDs also consume power as a result of signals switching inside the device. This power is often referred to as dynamic power.

The amount of energy consumed as dynamic power is proportional to the amount of processing undertaken. Thus, achieving an operation in 0.1 seconds at 100 MHz consumes approximately the same amount of energy (in terms of dynamic power) as achieving the same operation in ten seconds at 1 MHz.

These characteristics of dynamic and static power can be used to minimize the overall power consumption of a design by compressing required activity into a small time period and turning off the CPLD during periods of inactivity.
1. Overview of duty cycle approach.

For the duty cycle approach to work, the power up and down time of the CPLD clearly needs to be brief compared with the frequency at which the CPLD must be activated in order to achieve the desired processing and system response time. Fortunately, currently available CPLD devices utilize on-chip, non-volatile memory that yields power up and down times below 1 mS. This allows CPLDs to be activated at frequencies up to the low hundreds of Hz while still yielding useful power savings due to the duty cycling approach.

Implementing the switch

When implementing the duty cycle approach, it is necessary to engineer the design so that it is possible to turn the CPLD device on and off. There are several methods available to achieve this. However, the method chosen will be influenced by several factors. Key factors to consider include:

- The number of power supplies the CPLD has.
- What other devices, if any, share power supplies with the device.
- Whether devices sharing the same power supply rail can be duty cycled.
- The controls available within the power supply subsystem for disabling power supplies

There are three primary methods that can be considered when implementing duty cycling of the CPLD. The advantages and disadvantages of each method are described below.

**Use Power Supply Disable on the Voltage Regulator Module (VRM):** Many designs use VRMs to provide power to the chips within the design, and often these modules have a power enable/disable input signal that can be used to duty cycle the CPLD. The advantage of this approach is its relative simplicity. One disadvantage of this approach is its course grained nature, requiring all devices that are fed by the particular module to be cycled on and off at the same time. The second disadvantage is that the time required to power down and power up the VRM reduces the frequency at which the duty cycling can occur.

**Use FETs on the Power Lines to the CPLD(s):** In this approach FETs (Field Effect Transistors) are placed in the various power supply lines of the CPLD to be duty cycled. This approach has two key advantages. First, it allows specific device(s) to be duty cycled. Second, the power can be turned on and off very rapidly, which allows the device to be duty cycled at a higher frequency. The disadvantage of this approach is that additional devices are required on the circuit board, driving up
cost and board area.

**Use CPLD Sleep-Pin Functionality:** An increasing number of PLDs, such as Lattice's MachXO family, incorporate a "sleep pin" that allows the device to be disabled and the static power consumption reduced to almost zero. This functionality can be used to implement duty cycling. With this approach, only the specific CPLD is duty cycled and the turn on and off times allow for a high frequency of duty cycling. This approach also uses minimal components, saving cost and board area.

**Controlling the switch**

In addition to deciding what will turn the CPLD on and off, it is also necessary to decide what will control the switching operation. There are several options that are available, depending on the specifics of the system.

In many situations there is a microprocessor within the system. A general purpose I/O pin can be used to control the power supply. In many cases the microprocessor may also be turned off or placed in a sleep mode. In this case the CPLD can only be awake while the processor is operating. Care must also be taken to ensure that the pin used to control the CPLD power supply is well defined at all times during operation.

If there is not a microprocessor available, or if the CPLD is a critical part of the microprocessor subsystem that must be available prior to processor operation, then another device must be used. One option is to use a small zero power CPLD to provide the duty cycle control.

One typical approach is to have this device wake the main device. After the main device has completed its required processing, it signals that it is ready to resume sleep. Having received this signal, the smaller device asserts the sleep conditions. It then waits an appropriate length of time and reawakens the larger device. Many systems also have smart power supply management chips, such as one of the Lattice Power Manager series. These may also be used to perform a similar function.

If the input pin to the device switching the power supplies has hysteresis, then another alternative is a simple resistor capacitor timer. However, here it is important to consider the characteristics of the CPLD device when in the off state in order to avoid unexpected operation.

**Practical considerations**

Power supply cycling seems to be a great concept, but what other factors should be considered during the design phase? The first is how much power is consumed to power up the CPLD and then to power it down.

Based on previous experience with large FPGAs that often consume significant power in the form of in-rush current, most CPLDs draw only a modest amount of current during the power up cycle. *Fig 2* shows the power up characteristics of the Lattice Semiconductor MachXO device. As can be seen, energy consumption can be reduced by leaving the MachXO turned off for less than 1 mS.
2. Power-up characteristics of the Lattice Semiconductor MachXO.

Another key consideration is I/O leakage during the sleep phase. With CPLDs often having several hundred I/O pins, even a few microamps of leakage per pin can add up quickly. Key items to check include what voltages will be present on the I/O pins during the sleep mode, and what leakage the chosen CPLD exhibits under these conditions.

Another tip for reducing power consumption is to hold the inputs at a well defined 1 or 0 except when transiting. Typically even the best behaved device will consume additional power if the inputs are held at the threshold voltage.

Save some power today!
Duty cycling CPLD devices is a good method for saving power in applications where the CPLD activity can be compressed into small amounts of time. As noted, it is necessary to provide a method for switching the device's power supplies on and off. It is also necessary to decide how this switch is to be controlled.

There are also other practicalities to consider, such as I/O leakage while the CPLD is in the off state and the power draw while the CPLD is powering up and down. Fortunately, with forethought and careful component selection, these issues typically can be overcome, leading to lower power consumption in your next design.

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Gordon has been involved in the definition and launch of the LatticeECP / ECP2 / ECP2M FPGA families, the LatticeXP / XP2 non-volatile FPGAs, the MachXO family of programmable logic devices, and the ultra low power 4000ZE CPLD family. Prior to joining Lattice, Gordon worked in system
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