Design and analysis of a basic class D amplifier

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Introduction
In today’s world, power amplifiers are used in many devices for a wide variety of applications. In general, an amplifier takes a low power input and regenerates the signal at several watts higher. Ideally, the input will be reproduced without any changes with an efficiency of 100%. Various types of power amplifiers exist and they are classified by the amount of time that the transistors conduct.

Class A
Class A amplifiers are always turned on. This means that the transistor provides power to the output even when no input signal is introduced. Hence, the transistor can become hot with most of the power provided lost as heat. Although efficiency is poor (around 20%), accuracy is quite high.

Class B
Class B amplifiers use two transistors. Each transistor is turned on for half of the time. One transistor operates during the positive cycle of the input, while the other is used for the negative cycle. Therefore in theory, both are never on at the same time. When there is no input, both

Figure 1.1: Class A Amplifier
Transistors are turned off and no power appears at the output. For this reason, efficiency is better than class A amplifiers. However, due to the fact that transistors take some time to turn on, there is a moment when no power appears at the output. This powerless region is called the crossover region, as shown in Fig. 1.2, and introduces a relatively large amount of distortion. This class B amplifier has very good efficiency, but poor accuracy.

Figure 1.2: Crossover Region in Class B Amplifier

Class AB
Class AB amplifiers are very similar to class B amplifiers, but their performance is improved by the addition of two diodes that eliminate the crossover region and allows both transistors to be turned on at the same time. The efficiency (around 50%) is not as high as class B because both transistors are turned on simultaneously, but accuracy is improved. It is the most commonly used audio power amplifier.

Figure 1.3: Class AB Amplifier

Class D
Class D amplifiers are different from those mentioned above. The operating principle is based on switching transistors that are either fully turned on or fully turned off for a very short period of time. Both transistors are never turned on at the same time and hence very little heat is generated. This type of amplifier is highly efficient (around 95%). In the ideal case, it would be 100% efficient, whereas class AB amplifiers can only achieve 78.5%. On the other hand, the switching operation adds distortion to the output.

The improved efficiency of a class D amplifier makes it ideal for portable devices such as laptop computers and MP3 players. Class D amplifiers are not new, but recent advances in the technology of semi-conductor devices have regenerated interest in developing them. This basic design of a class D audio power amplifier discussed in this article was developed using PSpice to simulate the circuit. As part of the design process, the theoretical operation of the amplifier is analyzed and the physical amplifier tested in the lab. Comparison between simulation and experimental results yields some interesting points.

The amplifier is designed to provide an output of 5V to an 8 Ohm speaker, providing an output power of 3W. The amplifier should be able to pass all signals in the audio bandwidth (20 Hz to 20 kHz). At these frequencies, the gain should be constant with total harmonic distortion less than 1%.

**Class D Amplifier Operation**

Class D amplifiers consist mainly of 3 stages: the input switching stage, the power amplification stage, and the output filter stage.

For class D amplifiers to operate in switch mode, pulse-width modulation (PWM) can be used. This technique takes an audio input and converts it into a high frequency switching waveform. To achieve this, the audio signal is compared to a high frequency triangular waveform using a comparator as shown in Fig. 2.1. When the voltage at the inverting input is bigger than the one at the non-inverting input, the output voltage is low. When the voltage at the inverting input is smaller than the one at the non-inverting input, the output voltage is high. The output is shown in Fig. 2.2.

**Figure 2.1: PWM using a Comparator**
In class D amplifiers, the output of the comparator is connected to the power amplification stage. Metal-oxide-silicon field effect transistors (MOSFETs) are used at this stage instead of bipolar junction transistors (BJTs) because MOSFETs have a faster response time, ideal for high frequency operation. Class D amplifiers require two MOSFETs. They are either fully turned on or turned off for a very short period of time. When a MOSFET is fully turned on, the voltage drop across the transistor is small. When a MOSFET is turned off, the current across it is zero. The rapid switching of MOSFETs between these two stages makes it very efficient. Less power is dissipated as heat, thus a class D amplifier does not require a heat sink.

Class D amplifiers use two MOSFETs in a half bridge connection. These are the n-channel MOSFET (NMOS) and the p-channel MOSFET (PMOS). In order to turn a MOSFET fully on, it has to be driven into saturation. For NMOS, the gate voltage with reference to the source (VGS) has to be somewhat larger than the threshold voltage (VT 3V). A good value for VGS would be 5V since the MOSFET could be in its ohmic region for values between 3V and 4V. When VGS is equal to 5V, the MOSFET acts as a short circuit and no voltage is dropped across the transistor. All the voltage from the power supply is dropped across the resistor. When VGS is below VT, the MOSFET is cut-off and acts as an open circuit, therefore no current goes through the resistor and all the voltage from the supply is dropped across the transistor as shown in Fig. 2.3. For a PMOS, VT is negative (VT -3V). Therefore to turn the MOSFET fully on, VGS has to be more negative than VT (VGS -5V). To turn off, VGS has to be larger than VT (VGS > VT) as shown in Fig. 2.4.
Figure 2.3: NMOS
For this reason, an NMOS and PMOS connected as shown in Fig 2.5 will give a low output when a high input (VGS 5V) is present at the gate. When a low input (VGS -5V) is present, a high output will appear. The output of the comparator or input to the MOSFET (Vin) should be set to these two voltages to make sure that the NMOS and PMOS are fully turned on and off.
After the power amplification stage in a class D amplifier, a low pass filter is used to restore the original signal. A simple LC filter will convert the PWM signal back to its analog form with some added distortion. A speaker modeled by an 8 resistor is connected to the filter.

In summary, a class D amplifier consists mainly of 3 stages: PWM, power amplification, and a low pass filter. When these 3 parts are connected together, a simple model of a class D amplifier appears as shown in Fig. 2.6.
The main purpose of this project was to analyze and test a class D amplifier. A high power output was not necessary, but efficiency and distortion were considered. For these reasons, the components were chosen to reduce noise and improve efficiency.

Choosing the MOSFETs
When a MOSFET is fully turned on, a resistance appears between the drain and the source (RDS). For two MOSFETs connected in parallel as in Fig 2.5, it is important for the two transistors to have the same turn on resistance, otherwise the output voltage will not be symmetric as shown in Fig 3.1, which in turn will give a non-periodic output power as shown in Fig 3.2. In order to improve efficiency, it is recommended that RDS be smaller than 200m.

![Figure 3.1: Asymmetric Output Voltage](image1)

![Figure 3.2: Non-periodic Output Power](image2)

Fig 3.3 shows the delays present in a MOSFET. The turn on and turn off delays appear because the gate of the MOSFET needs time to charge and discharge. Once the MOSFET is turned on, the output voltage decreases until RDS reaches its minimum level (RDS(ON)). A low gate charge will reduce delays and improve efficiency and distortion rating. The gate charge should be lower than 20nC.
The MOSFETs used for the experiment were International Rectifier IRF520 and IRF9530. From the datasheets, it can be seen that both have RDS value of 0.20. For the low voltage level used in this experiment, both MOSFETs have gate charge smaller than 20nF. Furthermore, both can handle a maximum VDS of 100V and provide around 10A, which is quite sufficient for this design.

**Choosing the Comparator**

The comparator needs to be able to provide a positive output and a negative output. An ideal comparator would also be able to switch between these two levels instantly. However, due to its construction, a comparator needs time to turn on and turn off. Therefore, it is impossible to switch from high to low instantly. Consequently, when the switching time is small, the output voltage of the comparator will be stuck in the middle between high and low, unable to turn on or turn off the MOSFETs. When the PWM signal is converted back to its analog form, the signal will be distorted. In order to reduce distortion, a comparator must have a low propagation delay time. This will enable it to switch faster and operate at high frequencies. In Fig 3.4, a fast comparator is compared to a slower one with both of them operating at a high frequency. It is clear that the output of the fast comparator is a lot closer to the ideal case shown in Fig. 2.2 than the slower one. For this design, the MAX942 with a propagation delay of 80ns and a maximum output voltage of 6.5V was chosen.
Choosing the LC Filter

For a class D audio amplifier, the LC filter’s cutoff frequency \( f_c \), as shown in Fig. 3.5, should be set above the audio bandwidth. Furthermore, since the filter is used to convert the PWM signal back to its original form, \( f_c \) has to be determined with respect to the switching frequency of the amplifier, which is equal to the frequency of the triangular wave \( f_T \). Therefore \( f_c \) and \( f_T \) are related and both of these values will affect the amount of harmonics present at the output.

\[
\omega_c = \frac{1}{\sqrt{LC}} = 2\pi f_c
\]

Figure 3.5: Cutoff Frequency of LC Filter

For an input signal frequency \( f_s \), the lowest harmonic present is \( f_T - 2f_s \). Since \( f_s \) 20 kHz and in order to minimize distortion, it is required that \( f_T - 2f_s > 2f_s \), therefore \( f_T \) should ideally be 600 kHz. However, due to magnetic interference, a more practical value for \( f_T \) would be 300 kHz. Once \( f_T \) has been determined, only \( f_c \) remains to be established. In order to minimize the amount of ripple present at the output, \( f_c \) has to be smaller than \( f_T \). Therefore, \( f_c \) should ideally be equal to 20 kHz. Furthermore, \( f_c \) affects the amount of phase shift present at the output. A high \( f_c \) will decrease the phase shift, while a low \( f_c \) will increase it. For an LC filter, phase shift usually appears at frequencies above 10 kHz and brings delay in the microsecond range. Many researchers are still debating this question, but the importance of phase shift remains a perceptual issue that can only be determined by the listener.

For these reasons, the designer has to make a choice between phase shift and ripple. In this design, phase shift was considered. The LC filter is shown in Fig. 3.6 with its characteristics shown in Table 3.1. A higher inductance value will lead to an increase in phase, but it will reduce the amount of ripple. A higher capacitive value will also reduce the amount of ripple, but with less phase shift added.
Further improvements can be made by using a higher order filter, which will reduce the amount of harmonics without introducing a big phase shift [8]. A 4th order filter is shown in Fig 3.7, with its characteristics shown in Table 3.2. The output of the 2nd order filter is compared to a 4th order filter in Fig 3.8.
As Fig 3.8 shows, the 2nd order filter has more ripple, but less phase shift. The 4th order filter exhibits less ripple, but with more phase shift.

**Simulation Results**

To analyze the operation of the amplifier, the basic model shown in Fig. 2.6 was built and simulated using Orcad Capture and PSpice. The power supplies were set to 5V. Vcc and Vee were set to +5V and -5V. In order to facilitate testing in the lab, a 2nd order LC filter was used. Since phase difference appears at 10 kHz, a detailed analysis was made at that frequency.

Figure 4.1 shows the output of the amplifier. Several periods are shown on the left diagram. On the right diagram, a more detailed look illustrates clearly the harmonics present at the output. Also, it can be seen that the maximum output voltage is not equal to the supplied voltage. The gain of the amplifier can be calculated by \( \frac{V_o}{V_i} \) and is determined to be 4.
Figure 4.2 shows the Fourier analysis of the output. The fundamental frequency is located at 10 kHz and has a value of 4V. The significant harmonics are present at $f_T$ (300 kHz), $f_T-2fs$ (280 kHz), and $f_T+2fs$ (320 kHz). Harmonics are also present near $c$ (73 kHz) since resonance occurs at that point. Using PSpice, total harmonic distortion was calculated to be 0.71%, which satisfies the design requirements.

Figure 4.3 shows the average power absorbed, the power at the input, and the power at the output. The average DC power supplied is approximately 2W and the average power at the output is around 1W. Therefore, efficiency is around 50%, which is less than expected.

Figure 4.2: Fourier Analysis of Output with 10 kHz Input

Figure 4.3: Average Power Absorbed (top), Output Power (middle), Input Power (middle)

Figure 4.4 shows the MOSFET drain current. The series of impulses confirm that the MOSFETs are working in switch mode.

Figure 4.4: MOSFET Drain Current
Figure 4.4: PMOS Drain Current (top) and NMOS Drain Current (bottom)

Figure 4.5 (top) shows the output of the comparator with an observable turn on and turn off delay. Figure 4.5 (bottom) displays the voltage after the power amplification stage. The RDS(ON) delay is visible at this point. The output voltage of the MOSFETs is approximately equal to the supplied voltage. Therefore, from Fig 4.1 where the amplitude is equal to 4V, it can be concluded that there is a voltage drop at the output filter stage.

Figure 4.5: Comparator Output (top) and MOSFETs Output (bottom)

Experimental Results
To confirm the operation of the amplifier, the circuit shown in Fig 2.6 was built and tested in the lab. Fig 5.1 shows the output voltage obtained with an input sine wave of 10 kHz.
As Fig 5.1 shows, the simulation and the experimental results are different. In Fig 5.1, it can be seen that the output voltage is only positive, which means that the NMOS is never turned on. Fig 5.2 illustrates the output of the comparator with considerable delays present. Fig 5.3 displays the output of the comparator when it is disconnected from the rest of the circuit. From Fig 5.2 and Fig 5.3, it can be concluded that the comparator is not working properly when it is connected to the MOSFETs.

Figure 5.1: Output Voltage with Input of 10 kHz

Figure 5.2: Comparator Output
The variations between the experiment and the simulation exist because PSpice fails to model capacitive loading of the comparator MAX942. Due to the MOSFET’s construction, two parasitic capacitances appear at the gate. In order for a MOSFET to turn on and off quickly, a large current is required to charge the gate. In PSpice, the current that is supplied is approximately 300mA. However, according to the MAX942’s datasheets, the maximum output current that can be supplied is in the microamps range. Furthermore, it can be seen that as the capacitive load increases, the propagation delay rises. For a 500pF capacitive load, propagation delay is around 100ns. From IRF520 and IRF9530’s datasheets, it can be observed that their input capacitance is equal to 330pF and 760pF respectively. When connected in parallel, the total output capacitance seen by the comparator would be equal to 1090pF, which is very large in comparison to the comparator’s drive capacity. Nevertheless, when using PSpice, the comparator shows few delays even when connected directly to a 1090pF capacitor as shown in Fig. 5.5. Therefore, due to the differences between the comparator model in PSpice and in the design, the results obtained by simulating the circuit of Fig. 2.6 cannot be reproduced in the lab.
Second Model of the Class D Amplifier

Due to the comparator’s inability to support large currents as tested in the lab, a new model of the class D amplifier is needed. In order to quickly turn on and turn off a MOSFET, a gate driver can be used. Connected between the comparator and the MOSFETs, the gate driver can charge and discharge the gate capacitance in a short period of time.

A gate driver is able to reproduce a PWM signal since it functions at high frequency. However, most gate drivers can only provide positive output voltages, therefore only NMOS can be turned on by them. A gate driver for class D operation has to provide a high and low output voltage in order to turn on and off simultaneously two NMOS connected as shown in Fig. 6.1. When the PWM input is high, HO is off and LO is on. Only the bottom MOSFET is turned on, therefore the output voltage is zero. On the other hand, when the PWM input is low, HO is on and the LO is off. Since the top MOSFET is turned on, and the bottom one is turned off, the output voltage will be equal to the voltage of the power supply. LO is usually set to a value slightly greater than VT, therefore 5V would be correct. However, since the source of the top MOSFET is not connected directly to ground, HO has to be set higher in order to turn on the MOSFET. For example, if the supply is set to 5V, HO would have to be set to 10V. The connection shown in Fig 6.1 will reduce the amount of noise in comparison to the one shown in Fig 2.5 since the two NMOS connected can be chosen to be exactly the same, while it is usually difficult to obtain a NMOS and PMOS that have the same characteristics.
The gate driver shown in Fig 6.1 is a special type of MOSFET driver for class D amplifiers that provides both high and low outputs. However, most MOSFET drivers provide only an inverting output or non-inverting output. Nevertheless, using two gate drivers, the component shown in Fig 6.1 can be built.

A 2nd model of a class D amplifier is shown in Fig. 6.2. The TPS2811 and TPS2812 gate drivers provide an output voltage equal to their input voltage. In the case of the TPS2811, the output is inverted. Therefore, in order to provide a high output and a low output voltage, both gate drivers require PWM inputs at different amplitudes. For example, the TPS2811 require a PWM input with a peak to peak of 10V, while the TPS2812 require a PWM input with a peak to peak of 5V. The different PWM signals means that two comparators are needed. For this part of the experimental design process, the comparator used was the LM311 [12]. This was chosen over the MAX942, which is unable to provide an output of 10V.

Fig 6.3 shows the output of the circuit with an input sine wave of 10 kHz. The small peaks visible are
due to shoot through currents, which occur during dead time. Dead time is defined as the time it takes a gate driver to switch from on to off. Although distortions are present, this circuit is still an improvement over the results of Fig. 5.1.

![Figure 6.3: Output Voltage with Input of 10 kHz](image)

Fig 6.4 shows the input and output voltage of the gate driver for the high side MOSFET. As Fig 6.4 shows, there is more shoot through current present at the output. Fig 6.5 shows the input and output voltage of the low side gate driver. Once again, there is more shoot through current present at the output, but it is smaller than those seen in Fig 6.4. The increased current can be explained by the higher supply voltage required for the high side output. A higher voltage power supply will reduce dead time as shown in the gate driver’s datasheet. When dead time decreases, shoot through current increases.

![Figure 6.4: High Side Gate Driver Input (left), Output (right)](image)

![Figure 6.5: Low Side Gate Driver Input (left), Output (right)](image)

Fig 6.6 shows the output of the MOSFET. The delays visible are similar to those shown in Fig 3.3. Furthermore, the shoot through current is still present. Shoot through current cannot be eliminated since it comes directly from the construction of the gate driver. From the simulation, the turn on and turn off delays were expected. However, since PSpice does not model any MOSFET gate drivers, it is almost impossible to predict the effect of dead time and the resulting shoot through current unless tested in the labs. For this amplifier, when no input signal is present, the output voltage is 2V.
Efficiency can be improved if this value can be reduced to zero.

Figure 6.6: MOSFET Output

This amplifier can only provide a positive output voltage. However, if the bottom MOSFET was connected to a negative voltage instead of ground, the output would be as shown in Fig. 6.7, which is very close to the results obtained in Fig. 4.1.

Figure 6.7: Output with Negative Voltage Connected

In order for the bottom MOSFET to provide a negative output and to function in switch mode, the associated gate driver has to provide a negative output to turn off the MOSFET. Since the supplied voltage in this design is equal to -5V and VT is approximately 3V, the gate voltage has to be equal to -2V for the MOSFET to turn off (VGS < vt). Given that the tps2812 is unable to provide a negative output, it turns out that the bottom MOSFET is always turned on when a negative supply is connected instead of ground. This will not affect the shape of the output, but it will waste a tremendous amount of power. The mosfet stops functioning in switch mode and heats up quickly. Therefore, efficiency will be very low.

Conclusion
Using the first model, results from the simulations on PSpice confirmed the switching operation of the class D amplifier. The components used for the amplifier reduced as much as possible the amount of noise present at the output.
However, the first model of the class D amplifier did not function in the lab due to capacitive loading of the comparator MAX942, which is not modeled in PSpice. Since propagation delay is increased by capacitive loading, the comparator is unable to switch on and off at a high frequency. The second model of the class D amplifier solved the problem of capacitive loading by introducing the MOSFET gate driver. However, there is a significant amount of distortion at the output, which cannot be eliminated. Therefore, this model is not suitable as an audio amplifier. Improvements can be made by reducing delay time and eliminating shoot through current. Efficiency can be improved if the gate driver could provide a negative output voltage. In conclusion, the class D amplifier presented needs significant improvements before it can be used for audio purposes. However, Class D amplifiers have the potential to have 100% efficiency and therefore, are strong candidates as solutions for portable devices.

For more information