Preparing for a New Era of Growth in EDA

Luciano Lavagno and David Blaauw - May 09, 2002

Rather than dwell on the recent rough times in the electronics and high-tech industries, it's time we look ahead and prepare for the inevitable upturn. Companies that look toward a new era of design—examining upcoming trends, technologies, innovations and new markets—are certain to be in the forefront of this resurgence.

This year's 39th Design Automation Conference (DAC) will explore what lies on the horizon and beyond in the EDA industry. Attendees will find new ideas, methodologies and products that promise a bright future for design, and be exposed to new applications for existing tools. The technical programs planned for this year will explore significant issues in all areas of integrated circuit and system design, including the challenges of designing embedded systems, the re-emergence of analog design, and new approaches for dealing with increasing IC complexity, and power consumption and distribution.

For example, over the past several years DAC has become the premier forum for presentations and discussions regarding embedded system design. No one disputes that embedded systems are becoming a large part of the future of design. That is why one fourth of DAC presentations will be devoted to the questions and issues critical to the future of embedded technology. One session titled "Memory Management and Address Optimization in Embedded Systems" (Session 15) investigates new approaches for reducing and eliminating memory bottlenecks. "Embedded Software Automation: From Specification to Binary" (Session 23) explores advances in embedded software automation, including synthesis from synchronous specifications, automatic library mapping and the re-targetability of binary utilities. There are also several papers on "Processors and Accelerators for Embedded Applications" (Session 41) that explore the design challenges associated with taking an embedded application all the way to silicon.

If you're interested in the progress being made in tool and design flows for embedded systems, then plan on attending the panel discussion titled, "Unified Tools for SoC Embedded Systems: Mission Critical, Mission Impossible or Mission Irrelevant" (Session 31). In this panel, vendors, designers and members of academia will debate the future of SoC embedded design and the tools needed to get us there. Other areas concerning embedded systems will also be addressed at DAC, including new languages, hardware/software co-design challenges, power optimization issues, scheduling techniques, and design space exploration.

Analog design is once again entering the mainstream, with the explosion in communications products. A lack of designers with analog expertise and a very steep learning curve have led to a need for increased design automation in this area. The Holy Grail is to synthesize analog and mixed-
signal circuits. Progress is being made, but success may continue to elude the industry for some time. Several papers will be presented in this area, including Session 35 on “Advances in Analog Modeling,” and Session 29, “Analog Synthesis and Design Methodologies.” There will also be a panel discussion on IP issues titled, “Analog IP: Now? Or Never?” (Session 12).

Alongside these new developments in the industry, there is the continued upsurge in digital IC complexity. As chip complexity grows, the number and length of verification steps that need to be taken continues to increase. Formal and semiformal verification promises faster time-to-market through various new technologies and approaches being introduced, yet the learning curve remains steep. Can the current design environment continue to support existing methods, or will one of the new sets of technologies emerge as the leader? This topic will be addressed in various DAC panels and sessions, including a panel discussion titled, "Formal Methods: Getting Around the Brick Wall" (Session 37). IC complexity will also be addressed in several sessions on the breakthroughs in synthesis, cross-talk analysis, static timing, formal verification, equivalence checking, and simulation techniques. The program will also cover "Advances in SAT (satisfiability checking)" (Session 47) and "Moving Towards Effective Validation" (Session 50).

Power consumption and distribution is another roadblock for designers. Designers need smarter tools to address power and performance tradeoffs. A session on "Low-Power System Design" (Session 13) will present several ideas for minimizing power usage through dynamic voltage scaling. In Session 32, "Multi-Voltage, Multi-Threshold Design," you can learn new techniques for making tradeoffs between technology complexity, energy consumption and performance. Session 51, "Energy Efficient Mobile Computing," will explore power consumption as it relates to communication protocols, DSPs and CMOS. There will also be a session, "Low-Power Physical Design," that addresses new ideas for power optimization at the physical level (Session 30).

In addition to the focus on the technical aspects of design, there will also be several panels and special sessions that address current industry trends and future design possibilities. One panel will address the long-standing question, “Tools or Users, Which is the Bigger Bottleneck?” (Session 6). A panel titled, "Wall Street Evaluates EDA" (Session 1) will discuss the EDA industry's current unprecedented attention on Wall Street. Various constituents who play a role in shaping Wall Street's opinion of EDA, including representatives from top EDA vendors, analyst firms and trade publications, will discuss the current view of EDA by investors and analysts. They will explore why the sector is considered "hot" now compared to 2-3 years ago and the factors that have contributed to that perception. Another panel will explore answers to the question, "What is the Next EDA driver?" (Session 42). Several interesting special sessions will discuss, "Life After CMOS: Evolution or Revolution" (Session 7), "E-Textiles" (Session 11) and "Optics: Lighting the Way to EDA Riches" (Session 16).

This sampling of the presentations and panels underscores that the 39th DAC, June 10-14, 2002, in New Orleans will again be the center of intense learning and provocative discussion, helping prepare the electronics industry for a new era of growth. So don't miss this opportunity to stay connected, learn new methodologies and get a good look into the future of design.

About the Authors

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