The history of the EDA industry is punctuated by periodic upheavals in technology and consequently in the balance of power. Advances in semiconductor process technology and ever-increasing time-to-market demands are necessitating the re-creation of Electronic Design Automation (EDA) solutions. Key technologies such as synthesis are becoming commodities and the fundamentals on which traditional logical and physical design flows were built no longer apply. The current multi-vendor, multi-tool design flows can not adequately address timing convergence, nor handle multi-million gate designs. What designers really need is a single, integrated system that can take their design straight through the flow from RTL to GDSII with guaranteed performance.

Where will this breakthrough solution come from? The same place all the other EDA technology breakthroughs have come, from startups. Take synthesis, for example. Synopsys Design Compiler was a breakthrough 12 years ago, but until Ambit’s BuildGates came along, it had been virtually stagnating. BuildGates brought three major improvements to logic synthesis: larger capacity (up to 100K gates), better results during timing-dependent optimization, and time budgeting with a companion piece of distributed synthesis for very large designs. Synopsys responded to Ambit, its first real synthesis competitor, by making slight improvements to DC. But users are still stuck with the 12-year-old technology that DC was founded on.

Place and route has not so much stagnated as taken two steps back for every step forward. This is largely due to Cadence’s habit of acquiring decent technology, then bolting it onto its aging design flow rather than integrating it. This has created a profitable design service business for them, as it requires their experts to figure out how to make all the point tools work effectively together. But when was the last time Cadence actually developed a better, new place and route tool?

Fueled by their need to keep Wallstreet happy, both Cadence and Synopsys claim to have, or to be close to having, an RTL to GDSII flow that reduces iterations and addresses signal integrity and timing convergence. Not suprisingly, eliminating iterations, capacity for large designs and guaranteeing timing closure are not on their feature list. I commend them for their honesty because the truth is they can't deliver them.

The continuing reduction of feature sizes of semiconductor process technologies poses an insurmountable problem for these traditional synthesis, placement and routing systems. Most of these tools were developed 10-15 years ago when 10K gate designs were the norm, area was the toughest challenge, and interconnect delay was negligible. Back then the gap between synthesis and place and route was not a problem.
In today's DSM designs, interconnect wiring represents the majority of the delay in the circuit. Unlike gate delay, interconnect delay is difficult to predict during logic design because it is dependent on the final physical layout of silicon. As a result, with traditional EDA solutions, silicon design teams must perform numerous iterations between logical and physical design in order to meet timing, often delaying product releases by many months.

While Synopsys and Cadence have made big announcements about Physical Compiler and PKS—their current answer to the RTL to GDSII flow problem—they're really just repackaging existing synthesis, placement and global routing engines within a "synthesis" product. If these companies understood how to solve the problem and the needs of designers, they'd know that designers need tools that handle 1M- to 10M-gate designs, and that merely reducing iterations isn't enough.

To meet timing with these solutions, iterations are still required when placement estimates are invalidated by optimization and when parts of the design must be significantly restructured in a technology-independent fashion. In addition, the new solutions still require iterations between detailed placement and routing because they do not provide detailed floorplanning. Without detailed floorplanning these approaches must use guesstimates for macro and pad placement. The timing of a critical path between two macros consisting of only a few levels of logic is highly dependent upon exact macro locations.

Because these approaches cannot guarantee chip performance, designers benchmarking these tools will need to run through the entire chip design flow to GDSII. Only with DRC free GDSII, can a designer know if his chip meets timing.

These new solutions are also hindered by 100K gate synthesis capacity limitations. Placement and routing algorithms produce the best results with a flat design. In order to utilize these glue solutions, physical blocks are now restricted to the limits of synthesis, and hierarchy boundaries need to be defined based on tools' limitations. The serious problems with timing closure occur in 1M+ gate designs and are a direct result of long wires, macros, and pad placement.

To deliver a complete, integrated RTL to GDSII solution that eliminates iterations, guarantees timing, and has the capacity to handle large designs flat, logic and physical design technology must be completely re-designed. Synthesis must no longer rely on random wireload models or guesstimates of initial placement to manage interconnect delay. Synthesis must be tightly integrated with a complete physical design solution that uses timing as a primary constraint. To achieve the necessary level of integration, this solution must operate on a single, unified data architecture that allows the tools to work concurrently. Since Cadence and Synopsys clearly can not deliver such a solution, where is it going to come from? Without exception, startups have driven the technology advances that have changed the balance of power in the industry. If EDA history is any indicator, only a startup can offer this revolutionary solution.