Digital Receivers have revolutionized electronic systems for a variety of applications including communications, data acquisition, and signal processing. This series shows how digital receivers, the fundamental building block for software radio, can replace conventional analog receiver designs, offering significant benefits in performance, density and cost.

In order to fully appreciate the benefits of digital receivers, a conventional analog receiver system will be compared to its digital receiver counterpart, highlighting similarities and differences. The inner workings of the digital receiver will be explored with an in-depth description of the internal structure and the devices used. Finally, some actual receiver system implementations and available off-the-shelf board level digital receiver products for embedded systems will be described.

**Analog Receiver**

The conventional heterodyne radio receiver, as seen in Figure 1, has been in use for nearly a century. Let's review the structure of the analog receiver so comparison to the digital receiver becomes apparent. First the RF signal from the antenna is amplified, typically with a tuned RF stage, that amplifies a region of the frequency band of interest. This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator (LO) whose frequency is controlled by the tuning knob on the radio.

![Figure 1](image1.png)

1. Typical analog receiver block diagram.

The mixer translates the desired input signal to the intermediate frequency (IF). (See Figure 2.) The IF stage is a bandpass amplifier that only lets one signal or radio station through. Common center frequencies for IF stages are 455 kHz and 10.7 MHz for commercial AM and FM broadcasts. The demodulator recovers the original modulating signal from the IF output using one of several different schemes.
For example, AM uses an envelope detector and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio amplifier which drives a speaker.

2. The mixer translates the desired input signal to the intermediate frequency.

The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal. The frequency of the LO is set so that the difference between the LO frequency and desired input signal (the radio station you want to receive) equals the IF.

For example, if you wanted to receive an FM station at 100.7 MHz and the IF is 10.7 MHz, you would tune the local oscillator to: 100.7 - 10.7 = 90 MHz

This is called "downconversion" or "translation" because a signal at a high frequency is shifted down to a lower frequency by the mixer. The IF stage acts as a narrowband filter which only passes a "slice" of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or the "radio station") that you are trying to receive. For commercial FM, the bandwidth is about 100 kHz and for AM it is about 5 kHz. This is consistent with channel spacings of 200 kHz and 10 kHz, respectively.

**Digital Receiver**

Take a look at the digital receiver block diagram shown in Figure 3. Note the strong similarity to the analog receiver diagram; all of the basic principles of analog receivers still apply. Right after the RF amplifier and an optional RF translator stage, we use an A/D (analog-to-digital) converter to digitize the RF input into digital samples for the subsequent mixing, filtering and demodulation that are performed using digital signal processing elements.
Before we continue, let's first review a theorem fundamental to sampled data which lays the foundation for the A/D converter requirements. Nyquist's Theorem: "Any signal can be represented by discrete samples if the sampling rate is at least twice the bandwidth of the signal." For example, if we use an A/D converter sampling at 70 MHz, then the bandwidth of the analog input must be less than 35 MHz.

**Aliasing**

Now let's see what happens if we ignore Nyquist's criterion. **Figure 4** shows a frequency display of a system being sampled at frequency $f_s$. For all input signals below $f_s/2$, such as the one at $f_o$, we fully meet the Nyquist criterion. In fact, any number of signals can be present in the shaded region and all will be correctly represented in the sampled data.

But if we have a signal present at say, $f_a$, which is above $f_s/2$, the sampling process will generate an aliased image which will appear in the sampled data at $f_s-f_a$. This image cannot be distinguished from a true signal which might have been present at that same frequency. The point is this: once an aliased image is created in the sampling process, no amount of further processing can distinguish between a true signal and an aliased signal. Therefore, it is imperative to prevent aliasing before it occurs.

The most straightforward way to prevent aliasing is to use a low pass filter before the A/D converter which removes all signals above $f_s/2$. This filter, called an anti-aliasing filter, is seen in **Figure 5**. Now the signal at $f_a$ is blocked so the A/D converter never sees it. Anti-aliasing filters are often included on the same board as the A/D converter as a convenience to the user.
5. A low pass filter can be used as an anti-aliasing filter.

As a side note, Nyquist’s criterion can also be met by limiting the bandwidth of the sampled signal using other types of filters. For example, suppose we really wanted to receive signals between $fs/2$ and $fs$ in the above diagram. If we used a bandpass filter with a passband from $fs/2$ to $fs$, we would fully meet the Nyquist criterion because the bandwidth is equal to one half the sampling rate.

Once the sampling is done, the band of signals from $fs/2$ to $fs$ is “folded” into the frequency band from DC to $fs/2$. This half-sampling frequency is often called the “folding frequency.” This technique is sometimes called “undersampling” and while this works well in theory, care must be taken in actual practice to ensure that the A/D converter supports the higher input frequencies it must handle.

**Receiver System View**

Looking again at the overall block diagram, the digital samples coming out of the A/D converter are being fed to the next stage which is the digital receiver chip (in the dotted line), as shown in Figure 6. The digital receiver chip is typically contained on a single monolithic chip which forms the heart of the digital receiver system. It is also sometimes referred to as a digital downconverter (DDC) or a digital drop receiver (DDR).

![Figure 6](image)

6. The digital receiver device as part of the entire system block diagram.

Inside the digital receiver chip there are three major sections:

- local oscillator
- mixer
- decimating low pass filter

Note that the inputs to the digital chip are the digital samples from the A/D and the A/D sample clock. With a 70 MHz A/D, samples are fed into this chip and processed in real time at rates up to 70 MHz! We will now explore each section of the digital receiver system shown in Figure 6, starting with the digital local oscillator.

**Local Oscillator**

First, let’s explore the LO highlighted in Figure 7. It’s a direct digital frequency synthesizer (DDS) sometimes called a numerically controlled oscillator (NCO). This device is implemented entirely with digital circuitry.
7. The layout of the local oscillator circuit.

The oscillator generates digital samples of two sine waves precisely offset by 90 degrees in phase, creating sine and cosine signals. It uses a digital phase accumulator and sine/cosine lookup tables. Note that the A/D clock is fed into the local oscillator. The digital samples out of the local oscillator are generated at a sampling frequency exactly equal to the A/D sample clock frequency, \( f_s \).

It is important to understand that the output sampling rate is always fixed at \( f_s \), regardless of the frequency setting. The sine/cosine output frequency is changed by programming the amount of phase advance per sample. A small phase advance per sample corresponds to a low frequency and a large advance to a high frequency. The phase advance per sample is directly proportional to the output frequency and is programmable from DC to \( f_s/2 \) with up to 32-bit of resolution.

Using a 70-MHz sampling clock, the frequency range is from DC to 35 MHz and the resolution is well below 1Hz. The LO has very impressive frequency switching characteristics as shown in Figure 8. When switching between two frequencies, the digital accumulator precisely maintains the phase of the sine and cosine outputs for phase-continuous switching.

8. Frequency switching characteristics of an LO.

When the frequency is changed, what actually changes is the amount of phase advance per sample. This allows the local oscillator to perform frequency shift keying (FSK) and very finely resolved sweeps. Transients and settling normally associated with other types of local oscillators, such as phase-locked loop synthesizers, are eliminated.
The time it takes to retune the local oscillator is simply the time it takes to load a new digital frequency word (32-bit binary number) into a register, usually well below one microsecond. Some digital receiver chips employ a local oscillator with a built-in "chirp" function. This is a fast, programmable and precise frequency sweep which is very useful in radar systems.

*Part 2 in this series examines the mixer and filter as well as receiver implementations.*

**About the author**

Rodger H. Hosking is Vice President of Pentek and was one of the co-founders of the company in 1986. With over 26 years experience in the electronics industry, he is responsible for matching new technology to advanced signal processing applications and for the definition of new products. He designed the first commercial direct digital frequency synthesizer, and holds patents in frequency synthesis and FFT spectrum analysis techniques. Rodger has a BS degree in Physics from Allegheny College and both BS and MS degrees in Electrical Engineering from Columbia University. He can be reached at rodger@pentek.com.