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TEMPE, Ariz. — A team based at Motorola Inc.’s corporate laboratory has demonstrated a 512-bit memory array that integrates CMOS switching transistors with magnetic tunnel junction elements.

Motorola has high hopes for its magnetoresistive random-access memory (MRAM), which is moving from promising technological curiosity to something the company claims will enter commercial production in mid-decade. MRAM has advantages over conventional flash, DRAM and SRAM memory technologies, the company contends.

Motorola's demonstration re-affirms the company's place, along with IBM and Honeywell, amid a vanguard of U.S. companies driving MRAM progress, outpacing Europe and Japan.

The U.S. lead is attributed to past funding from the Defense Advanced Research Projects Agency (Darpa), but that money is likely to dry up within a year or two. At that point a commercial case will need to be made to complete the MRAM technology development and bring it to market, an industry observer said.

Saied Tehrani, the MRAM program manager at Motorola Labs, based here, said he expects embedded MRAM arrays to be in the sampling stage by 2004, and fully qualified in products by the following year.

MRAMs are non-volatile memories with fast access times and a small cell size. With no detectable wear-out mechanism and no need for charge pumps to erase or write the bits, MRAM is being touted as a replacement for flash and for DRAM. Tehrani called it "the universal memory."

The Motorola demonstrator array exhibits read and program access times of just 24 nanoseconds, putting MRAMs in roughly the same speed bin as slow static RAMs and making them much faster than DRAMs. The write times range, Tehrani said.

The challenge to building MRAM devices, he said, lies in sputtering very thin aluminum oxide films across a wafer without pinholes. Motorola Labs has used 6-inch wafers, with an aluminum oxide thickness of just 20 angstroms. Together with other material layers, the magnetic film thickness ranges from 30 to 60 angstroms.
"We have a lot of work to do to make this more repeatable, more reproducible. But I am sure we can take this to much higher densities," Tehrani said. "The cell size is much smaller than SRAMs and is comparable to DRAM."

The 512-bit array was fabricated with a 0.6-micron technology, but a 0.2-micron technology has also been used.

"Skepticism has turned into belief," said Jo de Boeck, group leader for magnetoelectronics research at the IMEC research center in Leuven, Belgium. "The next step is demonstration on a production vehicle."

De Boeck called Motorola's results "very convincing in terms of micromagnetics, reproducibility and uniformity for their magnetic cells." Moreover, he said that Motorola has "a road map for system-on-chip by the end of 2003, according to Darpa communications," with the Darpa funding itself scheduled to end somewhere in 2001 or 2002. "I am convinced their in-house road map is independent from the Darpa funding," de Boeck said. "In other words, they're serious about the technology."

Old hat

However, the creator of another digital memory technology has called the MRAM "old news."

"Honeywell, IBM and Motorola have been working on it for 10 years and yet you don't see any of the memory companies rushing to embrace it," said Richard Lienau, a technical consultant for Pageant Technologies, and inventor of a technology based on ferromagnetics. Called Magram, it combines non-volatility and random access.

Lienau said that any form of magnetoresistive technology is slow, difficult for building devices and requires exotic materials. Lienau's patents are owned by Pageant Technologies Inc. (Santa Fe, N.M.), a subsidiary of Micromem Technologies Inc. in Toronto. He plans to license the technology to memory makers.

IMEC's de Boeck, meanwhile, acknowledged that Europe has failed to keep up with U.S. progress in MRAM over the last couple of years.

Similarly, interest in MRAMs has hit a plateau in Japan, where excitement over ferroelectric memory has forced MRAM development onto a back burner. Two years ago, several Japanese memory makers began investigating MRAM when they learned that U.S. companies such as Motorola, IBM and Honeywell were building prototypes.

Many believed the Japanese could quickly catch up because of their expertise in manufacturing both memory devices and giant magnetoresistive heads for hard-disk drives. Yet more than a year later, it's unclear whether Toshiba Corp. or other Japanese companies are getting anywhere with MRAM.
"My impression is that it's considered the next step, because work is being conducted at our research lab and not in product development," a Toshiba spokesman said.

At one point, there was even talk of starting an MRAM national research project in Japan under the auspices of the Ministry of International Trade and Industry. That idea has apparently fizzled.

**Waning interest**

Kazuhiro Goto, executive adviser for the nonprofit research firm Asian Technology Information Program, said MRAM development work "is stopping" in Japan. Last year, Goto's firm published a report on MRAM research and made plans to host an MRAM conference in Japan, but the event was canceled due to lack of interest, he said.

Instead, Japanese companies are reemphasizing ferroelectric RAM, a technology that has been gestating for more than 10 years and has seen accelerating progress in sales and development in recent years. "The Japanese are focusing on FRAM, that's why [MRAM] work has been very slow," Goto said.

Along with Motorola, IBM Corp. has reported breakthroughs in its MRAM development efforts in recent months. IBM, which has been conducting MRAM research for three and a half years with the support of Darpa, announced in February that researchers at the Almaden Research Center in San Jose, Calif., had built a 1,000-cell MRAM array and integrated it with a CMOS circuit to be used for reading and writing to the MRAM.

IBM demonstrated that the device could obtain a read state in 2.3 ns and a write state in 3 ns. Researcher Stuart Parkin, one of three leaders on the MRAM project, told EE Times those speeds make the device almost as good as standard SRAM. Parkin said the device is already six times denser than conventional memory.

Since it began work in MRAM, Parkin said Big Blue has made significant strides in magneto structures, and has created a magnetic RAM with the largest difference between device states, the lowest resistance and the ability to be integrated with CMOS circuits.

For their part, researchers at Honeywell's Solid State Electronics Center in Plymouth, Minn., have been working on MRAM technology for 13 to 14 years, said program manager Hassan Kaakani, with funding from both Darpa (a three-year program that ends in 2002) and the U.S. Defense Threat Reduction Agency (DTRA).

Kaakani said Honeywell is testing a 1-Mbit MRAM that would be manufactured using radiation-hardened technology for space and satellite applications. The read/write speed has not been evaluated, but the design goal is less than 100 ns, he said.

Another project, under the DTRA contract, is development of a non-volatile memory to be embedded in ASICs. Kaakani said Honeywell hopes to achieve write speeds of less than 20 ns and read speeds
of 10 ns or less for this device.

Parkin at IBM said that the Almaden researchers were the first to use magnetic tunnel junctions (MTJs) three and a half years ago, when other companies were using giant magnetoresistance (GMR), an all-metal technology. They were also the first to use a cross-point architecture, he said, which enables a much denser device than with the GMR approach. After witnessing IBM's successes, Parkin said that Motorola, Hewlett-Packard and Infineon Technologies have all recognized the advantage of using the MTJ structure.

An MTJ is a sandwich of two atom-thick ferromagnetic layers separated by an insulating layer of aluminum oxide. To read the device, an electrical current is passed through the stack. The contacts are located on the top and bottom of the device. That makes for a denser part than the GMR approach, where current is passed through a device, from one side to the other, and contacts are on the sides.

When the ferromagnetic layers have a parallel magnetic orientation, the electrical resistance is low compared with an antiparallel orientation. Bits are determined to be on or off by detecting a change of 30 percent or more in the magnetic field, or magnetoresistive ratio.

"What we have demonstrated recently is that a large signal can be dependent on a 30 percent change in the absolute resistivity of the cell," said Motorola's Tehrani. "That is large enough to do a signal read."

In a presentation to the International Magnetic Conference in April, Tehrani said that "significant progress has been made in the past few years on MTJ structures. Spin-dependent tunneling, or MR, is a result of the change in available density of states in the ferromagnetic layers for spin-up and spin-down electrons when the direction of polarization changes from parallel to antiparallel."

**Uniform resistance**

Process uniformity is critical to advancing MRAM technology. An RF-produced oxygen plasma is used to oxidize an aluminum layer to form the aluminum oxide tunnel barrier. If the aluminum is overoxidized or underoxidized, the desired magnetoresistivity will not be achieved.

"Because of the exponential dependence on both aluminum thickness and oxidation time, producing MTJ material with good resistance uniformity over an entire wafer is challenging," Tehrani said. "However, with excellent aluminum thickness uniformity we are able to routinely obtain RA [resistance area] uniformity of 10 percent, 1-sigma, over a 150-millimeter wafer."

Meanwhile, FRAMs have beat MRAMs into production, as Fujitsu Ltd. churns out 1 million per month. FRAMs are being used in Sony's Playstation 2 and as IC-based cash cards for some game machines in Japan. Fujitsu plans to introduce later this year a 1-Mbit FRAM, developed in conjunction with U.S. partner Ramtron. Fujitsu is also looking at ways to integrate FRAM into system-on-chip devices, and considers FRAM a key technology differentiator, said Kazuya Kobayashi, general manager of the semiconductor global project management team.