ChipPAC readies poor-man's flip chip

Anthony Cataldo - February 21, 2001

ChipPAC readies poor-man's flip chip
SAN MATEO, Calif. — ChipPAC Inc. is about to roll out an inexpensive low-inductance flip-chip package that promises to bring the package now associated with high-performance processors into broader use with semiconductors such as digital signal processors, ASICs, memories and graphics processors, the company's chief technology officer told EE Times.

The low-cost flip-chip technology is one of several new packaging types expected from ChipPAC in the next year. Others will include a multitiered chip-scale package that can pack three to four chips vertically, said CTO Marcos Karnezos.

The flip-chip package uses gold-stud "bumps" instead of the more expensive solder bumps that are usually attached to the die in this package type. ChipPAC attaches the gold-stud bumps using conventional wire-bonding equipment for a fraction of the cost of assembling today's flip-chip packages, Karnezos said. The first gold-stud bump flip-chip devices are expected to ship late this year, he said.

Flip chips used in high-end microprocessors can be five to 10 times more expensive than the wire-bonded packages that house the vast majority of semiconductors, but Karnezos said the cost of the gold-bump flip chip will initially come in at less than 50 percent more than wire-bonded devices. "Our target is to get within 10 to 20 percent," he said.

Invented by IBM Corp. more than 30 years ago, flip chip is a method of making a more direct electrical connection between a chip's die and its package. Conductive bumps are placed directly on the die, which is then flipped over and connected to the substrate or lead frame. The bumps can be 50 microns high, whereas wires are typically 4 to 5 millimeters long.

The advantage of using these smaller bumps is lower signal inductance — less than 1 nanohenry, vs. 4 to 5 nH for wires — along with lower power/ground inductance and better signal density. Karnezos said the signal inductance for both the standard flip chip and the gold-stud flip chip is negligible.

In recent years, CPU makers like Intel and Advanced Micro Devices have migrated to flip chips because high-frequency microprocessors have the most to gain from this package. However, the cost has made the package prohibitive for most other devices.

Non-trivial costs
"MPU makers can pay for it, but the rest of the applications cannot afford it because the package is many times more expensive than the silicon," Karnezos said. "First there is the cost of making the bump itself. Then there is the assembly process of putting the bump onto the substrate and the design of the substrate. These are non-trivial."

ChipPAC aims to reduce the cost by using wire-bonding equipment modified for the gold-stud bumps in an existing packaging and assembly plant. Flip-chip packages today must be transferred to a special facility to "bump" the underside of the die, which accounts for much of the cost premium, Karnezos said.

"The advantage of this is that the cost is [only] marginally higher than wire bonding and the infrastructure is here," he said.

Karnezos said ChipPAC has four customers, which he declined to name, that are planning to use the new flip chip for DSPs, memory, ASICs, chip sets and graphics devices.

Among ChipPAC's publicly announced customers are Atmel, IBM, Lattice, Lucent, NEC, Qualcomm, Sony and Texas Instruments.

ChipPAC has been developing the low-cost flip chip for the last 2.5 years, and is about to transfer the technology to its production plant in Ichon, South Korea, near Seoul. The company is now in the process of adding production equipment so it can begin customer qualification next quarter.

Today, ChipPAC's flip-chip packages can accommodate up to 300 pins, and the company is aiming to get that up to 500. That will keep the packages out of the range of high-end MPUs, programmable-logic devices and graphics chips that typically require more than 700 leads.

But Karnezos believes there's a midrange of silicon devices with 500 pins or less that the flip chip can serve, as well as silicon germanium and gallium arsenide devices.

ChipPAC plans to provide the flip-chip technology to early customers that have their own packaging facilities, and will then license the technology to its competitors, Karnezos said.

**Thinness program**

Meanwhile, ChipPAC is working to reduce the thickness of semiconductor dice and packaging substrates in order to stack multiple dice into one package. Today's most common stacked-chip packages combine SRAM and flash memory and are used in cellular phones, but Karnezos said ChipPAC will soon be able to stack as many as four chips in one package.

The company is now working on a package that holds four discrete DSPs, which will divide signal processing functions into separate voice, video, data and communications task. "We're building engineering prototypes, and they should appear [in the market] a year to a year and a half later,"
said Karnezos, who declined to name the customer.