CMOS RF SoC design shoots for 60 GHz

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We will describe a potential design of a radio-frequency system-on-chip that is backward-compatible with a 60- and 5-GHz wireless local- (or personal)-area network system. The SoC can support a smart-antenna array operating at 60 GHz with multiple inputs and outputs that operate at 5 GHz using orthogonal frequency-division multiplexing.

Making millimeter-wave RF transceivers has always been a fine art. Since 1980, finline and nonradiating dielectric (NRD) guides have become popular for realizing hybrid transceiver modules. The former was first widely applied in the United States, with Europe following suit. NRD guides were invented by Tsukasa Yoneyama, who later designed and developed complete millimeter-wave NRD transceivers for various wireless communication systems in Japan. Both finline and NRD guides are not planar, so genuine mechanical designs are often a necessity. As a result of the advance in compound semiconductors, multifunction RF ICs at millimeter wavelengths have included more and more building blocks; also, flip-chip integration of RF ICs on planar substrates has become common practice.

All this millimeter-wave integration of RF transceivers, however, must carefully interface with antennas or filters, since waveguide discontinuity problems are often serious. On the other hand, CMOS RF ICs have gained popularity for 802.11a/b/g wireless-LAN devices and soon will dominate not only wireless LANs but cellular as well. With CMOS technology still tracking Moore’s Law, we expect CMOS 60-GHz wireless applications in the not-too-distant future.

The CMOS antenna array contains 2 x 4 radiating elements and measures 4.8 x 3.8 mm², which occupies most of the real estate of 5 x 5 mm² of the 60-GHz CMOS transceiver RF SoC. At present, the low-noise amplifier, power amplifier and subharmonic mixer (SHM) cannot be realized for 60-GHz designs using 0.25-micron CMOS technology. So for the time being, these components will have to remain external to the chip.

The SHM area is 1.3 mm² using a 0.15-micron high-electron-mobility-transistor pseudo-HEMT process, which results in approximately a 2-dB conversion gain with 5- to 6-GHz IF output. This SHM employs the synthetic quasi-transverse electric and magnetic (TEM) transmission lines for RF chokes, matching circuits and stubs. The spirals are for output matching to the 5-GHz industrial, scientific and medical radio band.

The compact SHM design is believed to be the smallest of its kind to date. The synthetic quasi-TEM line is known as a complementary conducting strip (CCS) transmission line (TL), which combines the microstrip and tuning septa in a periodical fashion, allowing greater flexibility in controlling characteristic impedance and slow-wave factor as limited by the IC process technology. The CCS TL is less sensitive to the compacted design, since it is more response-limited to meandering waves than the conventional thin-film microstrip.
When plotting the measured results of the CCS TL in IBM's 0.25-micron 1P5M CMOS technology with extrapolated data from 40 GHz to 60 GHz, the thin-film microstrip shows more attenuation than the CCS TL, although the CCS TL has a perforated ground plane close to the lossy silicon substrate. When CMOS technology is ready for 60-GHz wireless RF circuit designs, the CCS TL will be incorporated to fit the real estate of the RF SoC.

Additionally, the 700-micron-long CCS TL translates to an 11.5-dB loss per guided wavelength at 5 GHz. When normalized to guided wavelength, the TL in general exhibits greater losses because it has greater skin depth at lower frequency.

We developed the so-called active CCS TL, which is periodically loaded by a negative differential resistance circuit called a lambda diode. A similar concept has been applied to the design of cross-coupled differential oscillators at 5.23 GHz, where the CCS TL acts as a lossy tank resonator with its losses offset by the negative differential resistance, thus rendering stable oscillation at 5.23 GHz—only 40 MHz offset from the theoretical prediction. Currently, the active CCS TL is extended to make a CMOS microwave 3-dB hybrid that renders precise I/Q outputs for quadrature detection of the RF signals.

Thus, our new approach utilizes the synthetic transmission lines for designing a 60-GHz CMOS RF SoC. The measured and theoretical results reveal that the proposed guiding technologies can be applied to the design of millimeter-wave and microwave components on the lossy silicon substrate. The receiver for a 60-GHz/5-GHz wireless system has an antenna that can be realized using a waveguide-fed slot antenna array for eliminating the unwanted effects from the lossy substrate. The simulated results show the antenna gain to be 5.24 dB at 60 GHz, while the 3-dB beam width is 40 degrees at 25 degrees from the broadside of the antenna.

Another quasi-TEM CCS has been fabricated and measured on both gallium arsenide and silicon substrates. The measured results show the attenuation constant of the CCS transmission line to be lower than the conventional thin-film microstrip line in the millimeter-wave frequency band. The active CCS TL has also been used to realize the LC-free oscillator at 5 GHz, demonstrating the feasibility of designing the building blocks of the receiving system such as subharmonic mixer, 90 degrees hybrid and voltage-controlled oscillator in the microwave frequency band.

Based on the work in design description, we believe that making the single-chip RF SoC in CMOS technology will become a reality in the near future, when CMOS devices with gate lengths smaller than 130 nanometers become popular.

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