Conexant takes plunge for second DVB-S wave

Ronald Wilson - July 26, 2004

San Mateo, Calif. - When the digital video broadcast for satellite version 2 (DVB-S2) specification emerged last year, it was not the best of news for established silicon vendors serving the set-top box market. Changes in the specification forced a new round of complex silicon development for the set-tops.

The changes were driven by service providers’ need for more bandwidth. But to play in the new set-top-box market, silicon vendors found that they would need to design a new demodulator and a new low-density parity check (LDPC) error-correction unit. That’s no small task. Recently, STMicroelectronics let it be known that it was working on such chips.

But last week Conexant Systems Inc. (Red Bank, N.J.) announced live silicon for DVB-S2: the CX24116. The chip includes both a demodulator and a forward-error-correction (FEC) unit, both compliant with the new spec as defined by the Digital Video Broadcasting Project consortium (www.dvb.org).

On the front end, the chip required a new pair of fast 8-bit analog-to-digital converters to handle the incoming analog I/Q signals and pass them to the demodulator. The demodulator handles both quadrature phase-shift keying and 8PSK modulation schemes at symbol rates of up to 30 megasymbols/second.

The FEC block implements a concatenated LDPC/BCH (Bose-Chaudhuri-Hocquenghem) error-correction scheme. Both the decoder and the FEC block required new designs, said Conexant product director Manjit Gill.

In addition to the functional blocks, the chip includes an industry-standard 8-bit microcontroller, which acts as a programmable state machine, to implement fast signal-acquisition algorithms, and which executes the driver code for the chip. By moving the driver on-chip, Conexant has simplified the external driver interface and reduced the amount of real-time work that must be done by the set-top box's control CPU, Gill said. That frees the set-top's CPU for other tasks such as graphics.

The CX24116, produced in a 130-nanometer CMOS process by Taiwan Semiconductor Manufacturing Co. Ltd. and packaged in a 100-pin exposed thin-quad flat pack, is sampling now. In 10,000s, it costs $25 each.