Silicon nanowire synthesis is CMOS-compatible, claims Leti

Anne-Francoise Pele - October 07, 2009

PARIS — The Electronics and Information Technology Laboratory of the CEA (CEA-Leti) of France has demonstrated that the synthesis of silicon nanowire can be achieved at temperatures as low as 400°C by using a copper-based catalyst and an unconventional preparation method.

Leti researchers said their results contribute to bridge the gap between CMOS technology and the bottom-up growth of nanowires. The immediate effect is the possibility to add new non-digital functions such as sensors and advanced photovoltaics architectures to CMOS chip making processes.

Leti indicated that researchers have long assumed that oxidized metals are not suitable for nanowire synthesis, so they usually have tried to remove the oxide. Leti researchers adopted a different view and have achieved industry-changing results by oxidizing the copper catalyst and using the high chemical activity of this oxide to reduce synthesis temperature of the nanowires.

Eventually, Leti researchers claimed it is possible to grow silicon nanowires with a CMOS-compatible catalyst and at CMOS-compatible temperatures.

In a discussion with EE Times, Leti’s spokesperson explained: "Semiconductor nanowires are important potential building blocks of future technology. Several applications in electronics, biology, chemistry, renewable energies and optic have already been demonstrated but they still have to be transferred to the semiconductor industry. Here, the bottleneck is the nanowire fabrication itself which is not compatible with CMOS fabrication processes. CMOS-compatibility necessitates synthesis with compatible catalysts at low temperatures (T<450°C)."

He continued: "Vincent Renard has found a method to produce silicon nanowires in a CMOS-compatible way. The method is based on the discovery of the crucial impact of oxygen in the preparation of silicon nanowires with copper based catalysts which are CMOS-compatible. The crucial importance of oxygen in the chemistry of the produced nanowires is further illustrated by their evolution under conservation in ambient atmosphere. The tip of the nanowires rapidly transform to a dense-particle array in a silicon-oxide matrix."

Questioned by EE Times about the potential impacts on the IC market, Leti’s spokesperson declared: "There will be first the possibility of introducing logic in the interconnect layers. Indeed, our result can in principle allow to fabricate vertical transistors in vias. This would be an interesting step toward reconfigurable interconnect."

The spokesperson added: "We believe that the most important impact may be through the possibility of adding new functionality above ICs. The new functionalities range from chemical or bio sensors to mechanical nano-actuators and embedded solar cells to provide power to the circuits."
And looking ahead, Leti's spokesperson said the next step will be to demonstrate applications using this new material. For example, a sensor on top of an appropriate information processing IC.

The technology has not yet been licensed to a semiconductor company, noted Leti's spokesperson. Separately, CEA-Leti and the California Institute of Technology (Caltech) announced they will unveil their joint nanosystem roadmaps on Nov. 10 at Caltech, in Pasadena, Calif.

In 2006, Leti-Minatec and Caltech's Kavli Nanoscience Institute launched the NanoVLSI Alliance to collaborate on nanoscience at Caltech and in microsystems science and engineering at Leti-Minatec. Researchers from both institutions are working together to transform nanotechnology-based prototypes into robust, complex sensing systems ready for transfer to industry.

The alliance recently launched the Caltech-Leti Nanosystems Sponsor Program for leading industry players to accelerate the commercialization of its nanosystem innovations.