Lattice : High-speed ADC interface design is FPGA based

Henri Arnold - January 16, 2008

Lattice Semiconductor has announced its LatticeECP2™ and LatticeECP2M™ (“LatticeECP2/M”) FPGA interface reference design supporting the Texas Instruments’ ADS6000 family of analog-to-digital converters (ADCs). LatticeECP2/M FPGAs provide a high-speed glueless interface capable of acquiring 14-bit ADC data at rates up to 120 MSPS from the two to four serial channels found in ADS6000 ADC family devices.

Systems migrating to higher sample rate/resolution ADCs often require an FPGA with an interface speed of approximately 800 Mbps to bridge between existing hardware and the newer interface provided by the higher speed ADC. Previously, only more expensive, high-end FPGAs could satisfy this requirement. Now, the LatticeECP2/M FPGA family is able to provide these bridge functions in an optimally sized FPGA at a significantly lower cost. With the LatticeECP2/M FPGA devices, designers can focus on processing the ADC data within the FPGA and routing it to other parts of
their system without having to worry about the timing details of high-speed ADC interfaces.

To facilitate design verification, the default configuration of the reference design utilizes a new hardware interface card developed by Lattice to work with existing TI and Lattice evaluation boards. This complete hardware/software package gives designers a working model from which they can quickly create their own custom solutions.

“The combination of the LatticeECP2/M FPGA reference design and TI’s ADS6000 solutions boards provides a quick and cost-effective evaluation platform for receiver solutions targeting advanced communications, imaging, test and measurement and video applications,” said Heinz-Peter Beckemeyer, Manager of TI’s High Speed Data Converter product line. “The latest offering enables customers to reach the market fast with a cost-optimized FPGA and multi-channel ADC solution that combines exceptional speed, performance, size and power.”

“Previously, only expensive, high-end FPGAs could interface with ADC bus speeds greater than 600 Mbps,” said Stan Kopec, corporate vice president of marketing. “Now our customers can take advantage of the LatticeECP2/M FPGA’s 840 Mbps source synchronous interface to design their systems at a significantly lower cost without sacrificing performance or flexibility. Our free reference design will help our mutual customers reduce their time to market.”

About the Texas Instruments ADS6000 Family

The ADS6000 family consists of dual and quad, 12- and 14-bit ADCs available in speeds of 65, 80, 105 and 125 MSPS. Each device in the family delivers exceptional spurious-free dynamic range (SFDR), high signal-to-noise ratio (SNR), high IF capability and low power per channel. By incorporating single- or dual-stream serialized LVDS outputs, the devices reduce board space by sixty percent compared to previous CMOS output solutions.

About the LatticeECP2/M FPGA Family

The LatticeECP2/M family has redefined the low-cost FPGA product category by providing performance and features that typically are available only on competitive, more expensive high-end FPGAs. The LatticeECP2/M family supports logic densities from 6K LUTs up to 95K LUTs, has high performance DSP blocks, supports DDR2 memory interfaces at 533Mbps and up to 840Mbps generic LVDS performance. Some of the high-end features incorporated into the LatticeECP2M family include embedded SERDES I/O and the most on-chip memory in its class. The LatticeECP2M family supports up to 16 channels of embedded SERDES operating up to 3.125Gbps, as well as protocols such as PCI Express, Ethernet (1GbE and SGMII), CPRI and OBSAI. LatticeECP2M Embedded Block RAM capacity ranges from 1.2 Mbits to 5.3 Mbits, representing up to a 400% increase over competitive low-cost architectures.

The LatticeECP2/M and TI ADS6000 Interface Design Platform

The TI ADC interface card, available immediately from the Lattice website, enables the interfacing of the ADS6425EVM evaluation board directly with the LatticeECP2 advanced evaluation board. The reference design uses about 5% of the FPGA logic to transfer the ADC codes on the serial source synchronous bus to its embedded block RAM memory.

Pricing and Availability

The interface card, LFE2-H-IC-EV, is available immediately for sale on the Lattice website at a suggested price of $195.00.
The LatticeECP2 Advanced Evaluation board and ADS6425EVM boards are available now from Lattice and TI, respectively. For further information about the ADS6000 family or to request samples and EVMs (Evaluation Modules), see http://www.ti.com/ADS6425evm

**About Lattice Semiconductor**

Lattice Semiconductor Corporation provides the industry’s broadest range of Programmable Logic Devices (PLD), including Field Programmable Gate Arrays (FPGA), Complex Programmable Logic Devices (CPLD), Mixed-Signal Power Management and Clock Generation Devices, and industry-leading SERDES products.

Lattice continues to deliver “More of the Best” to its customers with comprehensive solutions for system design, including an unequaled portfolio of high-performance, non-volatile and low-cost FPGAs.

Lattice products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in communications, computing, industrial, consumer, automotive, medical and military end markets. For more information, visit http://www.latticesemi.com

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