Altia's human machine interface tools selected by Altera

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The folks at Altia say that their HMI (human machine interface) tools have been selected by Altera for use in the PARIS automotive infotainment development platform.

Jointly developed by Altera and TRS-STAR, PARIS is an FPGA-based platform that enables designers to develop and scale automotive infotainment systems. Altia, a proven solution in the automotive industry, provides best-in-class GUI development tools and outstanding expertise in embedded system development.

The Altia DeepScreen code generator produces deployable graphics code from the Altia Design GUI builder for the PARIS platform. The DeepScreen code generator is available in two versions for PARIS:

1. A software-based rendering solution which leverages Altera's Nios II embedded processor for all graphical operations.
2. A hardware-based rendering solution which utilizes the TES D/AVE graphics engine.

The first version allows developers to get the highest graphics performance without the added cost of hardware acceleration. The second version, the hardware-accelerated target, takes full advantage of the TES D/AVE Graphics IP and maximizes performance with parallel hardware/software processing. Both solutions allow for 2D, color graphics with a full set of rendering features – vector objects, bitmaps, text, alpha blending, and transformations like scaling and rotation.

The FPGA-based PARIS platform, announced in October 2007, is designed to enable the easy integration of pre-approved intellectual property (IP) from Altera and partners and facilitate the fast and efficient development of automotive electronics applications.

The PARIS platform features an Altera Stratix II FPGA and Nios II embedded processor. It also includes digital signal processing (DSP) and video and imaging IP suites, and support for the latest automotive networking standards such as CAN, MOST, LIN, and FlexRay. Once designed, the PARIS platform allows automotive OEMs to port their designs into a production-qualified CPLD or FPGA or migrate to a low-cost, high-performance HardCopy II ASIC.