Silicon-on-Insulator for Power-Semiconductors and Power-ICs

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Abstract

A Silicon-on-Insulator (SOI) process permits realization of 100-850V devices with very low on-resistance (13Ω-mm2 for 800V devices). Advantages of SOI comprise full dielectric isolation of each device, no latch-up, reduced parasitics, higher frequency, lower switching dissipation, ease of high-side operation, just to name a few. An area of concern is the higher thermal resistance of oxide for heat dissipation. Thin oxides were therefore chosen, and ESD tests showed, that the new material performs like bulk silicon in short transients. SOA for repetitive pulses or DC dissipation can be treated with an adapted thermal model for material, package and ambient. The modular process sequence shown in Fig.1 permits realization of 250V circuits with only 10 masks, but also 850V circuits with full 5V CMOS library both at ground supply and at positive rail with 17 masks. The process, now in full production, permits the most cost-effective implementation of various complexity levels from simple smart-power circuits to power-ICs with extensive signal processing either on-chip or as a multi-chip solution in a single package. High-temperature operation is feasible up to 300°C, much higher than conventional silicon, but the ease and low-cost production is maintained, unlike GaAs, GaN, or SiC materials.

1 Introduction

The steady increase of mobile electronics (laptop and handheld) brings more attention to light-weight, efficient power-conversion circuits, bot for charging the batteries and for stabilizing the supply voltages. Weight can often be reduced with higher switching frequency (improved energy storage in inductors), but efficiency is determined by parasitic resistances and capacitors. Figure 1 shows a simple half-bridge topology for down-conversion of a bus voltage for a resistive load.

Figure 1: A half-bridge topology.

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Charge is in this example transferred from the positive supply through the upper power device (high-side), coil and load onto a storage capacitor, and in the next half-cycle from there through load, coil and low-side switch to lower supply. The load gets therefore an exponential saw-tooth voltage and current, which at sufficient RL time constants and short pulse with can be approximated by a triangular signal with reduced peak voltages.

Besides the obvious (and often difficult to reduce) resistance of the storage coil, also resistance of the switches in on-state, leakage in off-state, and switching losses all contribute to the dissipation of this circuit. This paper will show, that Silicon-on-Insulator (SOI) has advantages in all three aspects of the power switch: on-resistance, leakage (especially at high temperature), and switching loss, all are lower than in comparable bulk devices.

2 SOI for integrated circuits and power semiconductors

The advantages of SOI for ICs have been broadly discussed, they contain amongst others reduction of junction area, reduction of parasitic capacitors, lowering of leakage currents especially at elevated temperatures, elimination of latch-up, possibility for dynamic threshold due to individual wells per device.

Most of these advantages also hold for power-semiconductors, but some are particularly important. The significant reduction in junction area reduces displacement currents during switching, a large contributor to switching loss. Additionally, the reduced junction area reduces leakage currents due to thermal carrier generation, extending the temperature range for SOI up to about 300°C. Such temperatures make an improved metalization necessary, due to increased contact migration of Si and Al. The elimination of latch-up furthermore permits the use of the body diode of DMOS devices, which in bulk devices would lead to latch-up due to minority carrier injection into the substrate.

3 State-of-the art in power-semiconductors

Numerous solid-state switches have been realized. Bipolar transistors were rapidly supplanted by SCR or thyristors, due to the high current drive required by the former. The absence of turn-off mechanism except for zero-current switching severely limited even those devices. The current work-horse is the DMOS transistor, where a relatively short channel controls current, and a large drift region assists in building voltage in the off-state. A derivative of this component is the insulated-gate bipolar transistor (IGBT), which delivers higher currents due to a built-in bipolar gain, at the expense of a higher source-drain voltage, thus giving a non-ohmic \( I_d \) vs \( V_{ds} \) characteristics. A further device of large importance is the JFET, which as a normally-on device is useful for voltage regulation and start-up circuitry.

The semiconductor of choice is currently silicon, due to the ease of manufacturing. Large-band-gap semiconductors like GaAs, GaN, and SiC offer higher breakdown fields due to reduced impact-ionization [1] and therefore smaller devices, but the more complex processing, also for surface passivation, more than offsets this benefit.

3.1 Vertical DMOS

Most discrete switches are realized as vertical devices. On top of the heavily doped substrate, which serves as collector, a thick epitaxial layer is necessary to form the drift region. In this epitaxial layer the body and source is diffused, possibly combined with trenches to improve channel density. Typical processes contain 50-70 \( \mu m \) epitaxy and 6-7 masks, to produce 600V nominal devices with 18\( \Omega \)-\( mm^2 \) overall specific on-resistance [2].
3.2 Lateral DMOS - RESURF

Both epitaxial film thickness and specific on-resistance can be reduced by applying the RESURF [3] principle. Both source and drain are now on the top surface of the silicon die, simplifying contacting and making lateral isolation of devices possible. This in turn permits the co-integration of logic gates, protection- and drive circuitry, as desired. A typical 600V device can be realized with 7-25µm epitaxy and 12 Ω-mm² specific on-resistance.

3.3 Thin-SOI DMOS – double RESURF

Further reduction of key performance parameters of the DMOS are possible by the SOCOS design in thin-film SOI [4-8]. In this case the RESURF principle acts on both top- and bottom-interface of the SOI film, allowing an optimal doping density throughout the drift region, making it shorter and better conductive. 600V devices have been realized with 7 Ω-mm² specific on-resistance. The thin SOI film is also easy to terminate laterally by oxidation or trench etching, making dielectric device isolation possible. As mentioned before, charge storage is minimal and switching assisted by built-in electric fields, which supports higher switching speed for a given dissipation.

![Figure 2: Cross-section of thin-film SOI high-voltage component.](image)

3.4 Super-junctions

Recently, super-junctions have drawn a lot of interest due to their still lower on-resistance. The very low on-resistance (3.5 Ω-mm² for a 600V device, [2]) comes at the expense of 7-9 epitaxial layers, each with its own lithography step and tight doping control. The device again uses the RESURF principle on both sides of the drift region, therefore allowing optimal doping density, but the large body-drift capacitance with the junction in-between limits high-frequency application. It is also not clear, if the 12-13 masks necessary, with the 40-60µm overall epitaxial layer and yield aspects due to tight doping control permit for economical production.

4 Process options

Philips Semiconductors B.V. offers discrete vertical DMOS commodity products, several lateral DMOS processes, and modular thin-film SOI processes. The discrete components are optimized for a given voltage specification, whereas the lateral DMOS processes accommodate a wide voltage range, and choice is more determined by circuit topology and special requirements on devices for peripheral circuitry. The SOI processes, A-BCD for 20-100V and up to 10A, and EZ-HV for 100-850V, 1A have a modular structure. Depending on circuit complexity, 7-17masks will realize from discrete power devices to power-ICs (PIC) with full 5V CMOS library support. This ensures the most cost-effective solution for different applications, from complex multi-chip solutions to minimum-size products. In a related activity, an RF process with integrated coils for very-low power applications is made available by Philips, Germany.
5 Conclusions

A complete range of processes has been presented for cost-effective realization of power applications, such as SMPS, battery chargers, lighting ballast, audio- and video-amplifiers has been presented. A novel material SOI proves advantageous for integration density and high-frequency applications. Extensive know-how in several application fields has been accumulated.

References