Altera Unveils HardCopy for Stratix

Murray Disman - July 01, 2003

The manufacturer says . . .
Altera HardCopy Stratix Devices Deliver ASIC Gain Without the Pain

Altera Offers Industry's Only Complete, Risk-Free Solution from Prototype to Production

San Jose, Calif.--June 23, 2000--Altera Corporation unveiled its HardCopy Stratix device family, the latest generation of low-cost mask-programmed devices. Harnessing a powerful FPGA front-end, designers can now directly target a high-volume HardCopy device at the very beginning of the design process using the new and distinctive design flow now available in Altera's Quartus II version 3.0 design software. HardCopy Stratix devices are the industry's only complete prototype-to-volume production solution for high-density designs, taking full advantage of the flexibility, features, and time-to-market benefits of Altera's industry-leading Stratix FPGAs. Offering up to a 100 percent performance improvement over the FPGA, HardCopy Stratix devices deliver all the ASIC gain without the pain, minimizing the high development costs and long design cycles associated with ASICs.

Compared to the original HardCopy APEX devices, the new HardCopy Stratix devices delivers higher performance, lower power consumption, and a 30 percent cost reduction for equivalent logic functionality. With this announcement, Altera continues to meet the needs of system manufacturers who today are under tremendous pressure to meet both technical and business objectives.

Efficient channel coding, for example, has successfully integrated HardCopy APEX devices into their high-volume iPSTAR satellite modem, which will be deployed to millions of homes in the Asia-Pacific region. Mark Vanderaar, CEO of the company, said, "Altera's HardCopy solution delivered exactly what we had planned: a low-cost realization of our advanced satellite receiver technology. The day we received our HardCopy prototypes, we dropped them into the FPGA sockets on our iPSTAR satellite Internet modem product, and they worked perfectly. The HardCopy process has enabled our team to quickly and cost-effectively get to low-cost volume production."

Higher Performance, Lower Power Consumption, and Lower Cost

System manufacturers targeting a HardCopy Stratix design have the option to stay within their original performance targets, or boost performance by an average of 50 percent[]and in some cases, up to 100 percent. Power consumption also decreased up to 40 percent. Altera focused on lowering costs to assist customers in meeting their system cost targets. By targeting further efficiencies in the structure of the logic elements (LEs) and routing of the HardCopy Stratix architecture, additional cost savings of as much as 30 percent vs. the original HardCopy APEX devices were achieved for equivalent functionality.

"Altera's HardCopy Stratix solution offers significant differentiation from other products, which was a critical factor in our decision to partner with Altera," said Kuldeep Sandhu, co-founder, president
and CEO of Maranti Networks. "The HardCopy option allows Maranti to enter the market quickly with Stratix FPGAs, and then migrate to HardCopy devices to manage costs. This solution eliminates much of the risk and significantly shortens our development cycles, giving Maranti a competitive edge."

"Many designers today have been on the hunt for an alternative to their traditional ASIC solutions, but have been limited by price, performance, and power consumption. Not anymore," said Tim Colleran, vice president of product marketing at Altera. "HardCopy Stratix devices give both ASIC and FPGA designers the unique ability to leverage all the benefits of programmable logic and also reach the price and performance targets they traditionally could only achieve with ASICS."

**Seamless Migration**

The HardCopy Stratix devices retain the same advanced features as Stratix FPGAs, including hierarchical clock structure, TriMatrix memory, and optimized embedded digital signal processing (DSP) blocks. Like the Stratix device family, HardCopy Stratix devices support the same wide range of high-speed interfaces including SPI-4.2, 10 Gigabit Ethernet (XSBI), and the RapidIO standard as well as a variety of high-speed I/O standards including the LVDS, LVPECL, and HyperTransport standards. This enables a risk-free, seamless migration.

**Unique Comprehensive Design Flow**

What makes the HardCopy Stratix design flow unique is the ability to target a HardCopy device at the very beginning of the design process while taking full advantage of the performance and power improvements associated with Altera's HardCopy Stratix devices. From the very start, designers can verify timing, performance, and power estimates from within the Quartus II version 3.0 design software, based on actual logic placement on the HardCopy Stratix device. All of this capability is available in a $2000 suite of design tools that is already available to tens of thousands of engineers. ASIC designers looking to lower their total cost of ownership and get their product out quicker than ever before can now design to win with the new Quartus II software.

**State-of-the-Art Technology—Only from Altera**

All of Altera's HardCopy devices are based on a universal base-array with the same architecture as their FPGA counterpart. Only the top two metal layers are customized to implement the customer's design. Architectural enhancements in HardCopy devices include shorter path routes, reduced die size, and the removal of the silicon overhead associated with FPGA programmability, resulting in a 60 to 70 percent die size reduction compared to the original Stratix FPGA device.

HardCopy Stratix devices are manufactured on the same reliable, state-of-the-art 0.13 µm CMOS process as Stratix FPGAs. In partnership with TSMC, the world's largest wafer foundry, Altera continues to be the only FPGA vendor to ship the most advanced, all-layer-copper, 0.13 µm products in volume.

**Availability and Pricing**

The HardCopy Stratix device family includes five members ranging in density from 25,660 to 79,040 LEs. All devices are available in FineLine BGA packages. Customer designs will be accepted starting in Q3. Pricing is a function of the package option, device performance, and volume. Future volume pricing will range from $25 to $120.

**About Quartus II 3.0 Software**
Altera's easy-to-use Quartus II design software is the most efficient, comprehensive environment available for designing CPLDs, FPGAs, and HardCopy devices. The Quartus II design software includes a suite of advanced system-level design features, access to Altera's extensive intellectual property portfolio, an advanced place-and-route engine including physical synthesis optimization technology, and comprehensive verification solutions.

In addition, the latest third-party EDA synthesis and verification flows have been integrated into the Quartus II design software. For more information about the Quartus II design software, visit www.altera.com/software. Designers can also download Altera's no-cost Quartus II Web Edition design software at www.altera.com/q2webedition. Murray Disman says . . .

Times, they are a "changin" as the programmable logic vendors move away from their PLD base. Xilinx and Lattice Semiconductor (see Lattice Announces 10 Gbits/s SerDes) have introduced 10 Gbits/s ASSPs, and Altera has announced their move into the structured ASIC business. Altera does not like to call their offering an ASIC, but if it quacks . . .

All of these moves are based on internally developed technologies, and make a great deal of sense. Although the three companies will be able to sell the new products to current customers, Altera's approach is applicable to a much broader base of applications than the ASSPs from Lattice and Xilinx. It seems very likely that the structured ASICs being offered by Altera will add substantially more to the company's top and bottom lines than the 10 Gbits/s ASSPs will for Lattice or Xilinx.

It is hard to tell whether Altera got into the structured ASIC business through the back door or if the strategy was developed along with the planning for the Stratix family. The company implies that the back door was used.

Altera has been providing HardCopy conversions of its APEX 20KC, APEX 20KE, and APEX II devices for some time. These HardCopy parts usually contain elements that are used to slow performance to match that of the FPGA to avoid timing errors. The rational for the conversion was based strictly on cost savings.

The most recent HardCopy program was aimed at the conversion of designs executed in the APEX family of devices. According to Altera, some ten to twenty customers have converted APEX designs to HardCopy versions. Most of these conversions were for the larger APEX parts and typically involved production quantities in the 5K range. A saving of at least $1000 per part makes the conversion effort worthwhile.

Altera has identified three reasons that were behind a HardCopy customer's decision to convert an FPGA design. These were for production runs, as a bridge product to use while their ASIC was being developed, and as insurance against slippage in the ASIC development program.

HardCopy is aimed at the conversion of the larger chips in a family. HardCopy Stratix, for example, covers five chips with densities ranging from 25K to 79K logic elements. The entire Stratix family contains seven devices with densities ranging from 10K to 79K logic elements. The EP1S120 with 117K logic elements, which was announced when the family was introduced, has disappeared from Altera's current literature.

HardCopy Stratix is a Stratix device minus the elements that allow programming of the logic and routing, and the SRAM that stores the configuration data. This results in a reduction of 60% to 70% in chip size that leads to a price of a HardCopy part that is about one-third the price of the equivalent FPGA. The customer's design is implemented in HardCopy with two metal layers. The final two metal layers are then applied for power and clock distribution. These last two layers are identical for all designs, and the customer does not have to pay for these masks.
Feedback from Stratix customers about HardCopy indicated a desire for lower costs, higher performance, and lower power, with higher performance being the most important. HardCopy devices are inherently faster than their FPGA counterparts. It could have been at this point that the lights went on—why not offer a solution with improved performance, as well as a lower cost?

In order to verify performance capabilities, Altera ran about 100 customer Stratix designs targeting a HardCopy device. The performance results ranged from almost no gain to an increase of 110%. Minimal gains occurred for those designs that made extensive use of the hard IP in the device—the MACs and embedded memory. The best gains were seen for those designs that were routing dominated. The average performance increase was 50%.

Looks like the company got a two-for-one bargain when they tied two approaches into a single software solution with a new release of its Quartus design system. Altera was able to preserve the traditional HardCopy migration route for those customers satisfied with the FPGA's performance who are only interested in reducing costs. The second, more interesting result, facilitated the move into the structured ASIC business.

The customer could now do an FPGA design and automatically produce a HardCopy design. Either or both designs could be altered independently to reach the desired performance levels. The other approach is to do and optimize the HardCopy design first and then automatically produce the FPGA design. The resulting FPGA could then be used as a prototype of the design. All of this can be accomplished with Altera's $2000 Quartus design package.

Is there really a structured ASIC business? Well—it’s not much. NEC, one of the key participants, revealed that it had executed all of 20 designs for its ISSP structured ASIC product since it was introduced. Lightspeed may have done more. Still, I doubt if more than 100 structured ASIC designs were completed last year. In addition, a similar number of FPGA conversions were probably done using a structured ASIC as the targeted platform. This represents, at best, 10% of the number of ASIC design starts last year and 2% of the number of ASIC starts during the good old days.

Structured ASICs possess neither the performance nor the density of a cell-based ASIC. However, they do offer a very promising middle ground between the very high development cost of a cell-based ASIC and the very high unit cost of the larger FPGAs. Altera may have struck gold with HardCopy Stratix.