INTRODUCTION
As a concept, “System in Package” or “SiP” relates to the objective of merging many or all of the electronic requirements of a functional system or a subsystem into one package. It is a concept that can at once be understood by people familiar with electronics and packaging yet is very difficult to define in absolute terms. Amkor uses the following attributes to define SiPs:

- Includes chip-level interconnect technology. In other words flip chip, wirebond, TAB, or other interconnect directly to an IC chip. This distinguishes small SMT board assemblies from being considered SiPs.
- More often than not, the SiP is small in physical size.
- Quite often includes passive components. The passives can be either surface mounted discrete components or can be embedded into or manufactured on the substrate material.
- Typically includes more than one IC chip.
- May include other components necessary to bring the SiP to a more complete functional system or subsystem level – such as housings, lids, RF shields, connectors, antennas, batteries, etc.

Quite often the term System-in-Package is used to describe multi-chip IC packages such as stacked die CSPs or MCM-PBGAs. The real power of SiP technology lies in its ability to integrate not only multiple ICs but also other components such as passives, connectors, antennas and so on into the package in order to create fully functional subsystems.

System in Package has a parallel in the often-discussed System on Chip (SoC) methodology. While SoC has many good attributes, and has been the focus of several IC manufacturers for several years, by its very nature it is limited by what can be achieved within one wafer process. It is quite easy to understand that SoC may be limited in the type of IC functions that one would like to design into a system – or at best performance will likely be compromised due to a common wafer process. SiP is not limited by the constraint of a common wafer process, so that IC chips, each optimally suited for its function by both design and wafer fab process, can be easily combined together in one package (for example a CMOS digital IC with a GaAs HBT RF IC).

There are several reasons why the market demand seems to be growing strongly for SiP solutions. These include:

- Size: The size of sub-system can be reduced by integrating multiple ICs and other components in an SiP
- Time to market: It is often faster combine ICs in a SiP than it is to implement SoC at the IC level. It is also faster to make changes to the system at the SiP level than to change the entire mask set of an SOC solution. SIP implementation is faster than tune & debug at system board level, especially in RF applications, (e.g. cell phones)
- SiP solutions reduce the complexity of the motherboard by moving the routing complexity to the package substrate. This often results in reduced layer count in the motherboard and simplifies product design.
- Performance advantages: – e.g. ASIC or CPU to memory data speed enhancements by combining the logic and memory chips close to one another in the SiP. Another example is power reduction by minimizing line lengths (capacitive loads) between IC’s in a SiP.
- For RF & Wireless SiPs – the package is literally a part of the circuit and the package design and materials selection can have a great impact on whether the RF circuit functions as intended.
- Fully integrated “plug and play” SiP solutions enable system designers to implement additional functions, such as Bluetooth or camera modules, into a system with minimal design effort.
- Lower System Cost: An optimized SiP solution usually results in an overall system cost reduction compared to discrete IC packages.
- SiP enables the system designer to mix and match IC technology in order to optimize the performance of each functional block. Note that SoC and SiP are not mutually exclusive, but SiP offers more flexibility in IC partitioning to optimize performance and cost.

SiP APPLICATIONS
SiP technology has its roots or heritage in both IC & SMT technology. But although there are some similarities, SiP does not really share very much history with either hybrid components or high performance
MCM’s developed in the past. When one generally thinks of hybrid technology, the thought is often of modules that are expensive to manufacture (often using expensive ceramic substrates) and typically low volume. MCM (MultiChip Module) technology has been previously used for high performance applications like mainframe CPU’s (found, for example, in Fujitsu or IBM mainframe computer systems). These type of MCMs typically are very complex and very expensive (e.g. the MCM used for the IBM 4300 computer used a glass-ceramic substrate with more than 40 layers and containing more than 25 IC’s).

SiP has not borrowed much from the hybrid or MCM history, but is based more on a merger of mainstream, high volume, and low cost IC assembly technology and surface mount technology. The IC assembly technology is used to interconnect the IC chips to the SiP substrate while the SMT technology is used to connect passive components and other SMT-compatible components (e.g. connectors) to the SiP substrate.

SiP builds strongly on existing technology (materials, equipment, and process flows) to keep the SiP cost low and also to allow support of high volume manufacturing as SiPs are more widely adopted in the industry.

RF/Wireless SiP Applications

Today’s wireless market is largely driven by the cell phone industry where cost, size, performance and time to market are the primary driving factors. Many companies, such as Ericsson and Motorola, are moving from being vertically integrated to outsourcing the manufacturing of the phone. With increased OEM outsourcing and the “built-in-China” content requirement for that emerging market, the building of cell phones is being provided by less engineering sophisticated manufacturers, thus driving a need for simplification of the RF functions, ease of assembly and/or increased skill sets from the manufacturers. The phones themselves must support higher data rates for 2.5G and 3G and must also take on additional applications such as Bluetooth, while at the same time maintain cost parity and achieve the same performance in a smaller volume. Time to market continues to be a dwindling parameter as the introduction of “smaller, thinner, lighter and with more functionality” becomes a competitive edge.

Bluetooth, as a separate wireless market, shares many of the same requirements as cell phones due to the cost sensitivity of the solution set. The Bluetooth SiP market can be segmented into three general groups:

- **RFIC only.** In this case the host application absorbs the DSP function into a larger baseband function (Cell phones) and the RFIC is typically contained in a discrete semiconductor package.
- **Full function, single chip and multi-chip solutions** that integrate RF and baseband functions as well as flash memory in a single module. There are many different approaches to IC segmentation and, as a result, a variety of SiP solutions.
- “**Plug n’ play**” solutions with the antenna integrated into the module. This latter segmentation also falls into the category of “users with little to no RF capability”, but whom want to add Bluetooth capability to their products. Bluetooth IC solutions, being primarily designed in CMOS most often have balanced transmit and/or receive I/Os requiring a recombination of these signals in a balun. For full functionality all of the IC’s require a band pass filter and shielding in order to meet Bluetooth requirements as well as regulatory requirements.

Bluetooth will serve a number of markets of which the cell phone is one. For the Bluetooth product developer with little or no RF experience a “Single Component Radio” will be necessary to facilitate rapid time to market of new applications. This entails including the antenna, shield, supporting circuitry and die (or multi-die) within the package. A Bluetooth component of this type is currently in development and is being co-designed by Amkor with a customer.

In the cell phone market the trend appears to be the modularization of the phone first into 3-4 modules and moving towards a single cell phone module. The first use of SiP is in the power amplifier stage of the transmit chain. Previous PA solutions were discrete implementations with matching and control circuitry on the motherboard. Today’s SiP PA solutions provide controlled impedance I/Os for the RF with all matching internal to the SiP, greatly simplifying the manufacturers operations and rework. SiPs can be found as both laminate and ceramic solutions, however most solutions are moving towards a laminate implementation. In the near future, SiP will include integrated shielding in the PA further simplifying the assembly and logistics for the manufacturer.

![Figure 1 Typical Dual band RFPA system-in-package circuit containing 2 GaAs die and passive components on a 2 layer laminate substrate.](image-url)
Following the PA there are a number of manufacturers who are looking to integrate the baseband function of the cell phone. Typically the baseband engine, SRAM, Flash and the BAI, along with a number of passives will be integrated. The desire here is to have an engine that can quickly be configured with changes in the analog front end to provide rapid product changes. Reduction in area is a prime concern resulting in the use of stacked die as an area reduction technique. It is possible to stack 2-3 die depending upon thermal and routing considerations. Such a baseband SiP that moves most of the system routing complexity from the motherboard to the SiP substrate can now have a larger BGA pitch (1.0 or 1.27 mm) compared to the typical BGA pitch of individual packages for each component (0.5-0.8 mm). This will simplify the manufacturing requirements of the OEM and reduce motherboard cost and complexity.

The entire Transmit and/or Receive chains are next in line. At this point, this is being divided between the transmit and receive sections in order to maintain isolation between the sections. Amkor has developed internal module shielding which holds the promise of meeting the isolation and regulatory requirements. However, this area is likely the last to be integrated due to the complexity of the RF circuitry and the desire by product developers to keep internal the “RF Knowledge”. A strong understanding of the RF/Microwave characteristics of substrates, embedded passives and structures and design techniques is critical to any circuitry involving the assembly and test of these functions.

Sensor Applications
Recently there has been explosive growth in the use of Si-based sensor technology for a variety of applications including biometric sensors (e.g. finger print sensors) CMOS image sensors, and MEMS sensors, such as accelerometers. Increasingly, sensor devices are being integrated into portable devices like handsets and PDAs. In these applications small size, low cost and ease of integration are key to successfully integrate sensor technology. OEMs generally want a plug-and-play module, or complete subsystem, containing not only the sensor itself but also the control IC and circuitry.

State of the art CMOS image sensors contain up to 3.17 mega-pixels on a single sensor die. Commonly, CMOS image sensor die are packaged in a discrete package such as Amkor’s VisionPak LCC (fig. 2). This package provides a leadless chip carrier with a clear protective cover for the sensor die. A separate package is required for the driver IC and the lens must designed and assembled by the OEM or a third party subcontract assembler.

Figure 2 VisionPak™ CMOS image sensor package
Within the last year there have been many implementations of CMOS image sensors in portable products such as mobile phones. In these applications it is necessary to minimize size and cost. Module solutions that can simply plug into the cell phone motherboard are required. Using SiP technology we can enhance a standard VisionPak™ package by integrating the lens assembly. This has the advantage of much more accurate placement of the lens with respect to the sensor die, and enables the use of simplified fixed focal length lenses. In addition, the driver IC can be mounted on the bottom side of the SiP substrate along with passive components. A flex connector can be added for easy assembly to the handset motherboard.

Figure 3 Fully integrated CMOS image sensor system-in-package solution containing lens assembly, driver IC passives and optional flex connector.

Networking and Computing Applications
SiP technology offers many of the same benefits for high-speed digital devices. Many applications in the networking/computing market require integration of memory devices with ASICs or microcontrollers. For example, graphics modules for PC chip sets typically
include a graphics control IC and 2 SDRAM devices. Today, most graphics modules are manufactured in a standard MCM-PBGA format. This approach is cost effective from a packaging standpoint, but the memory die present some unique challenges. The SDRAM devices require a full dynamic burn-in. However, cost effective wafer level burn-in processes have not been developed and deployed for SDRAM devices yet, so most suppliers are selling SDRAM wafers that have only been through a static burn-in. So there is a potential for yield loss when bare die SDRAM is assembled in a module format. In MCM format it is usually not possible to test the DRAM directly – memory must be accessed through the graphics chip at final test. Similarly, the graphics chip can’t be fully tested independently. Therefore, it is often difficult to determine the exact source of a failure that occurs at final module test.

In packet switching applications for internet routers there is typically a high pin count ASIC device that is in communication with up to 8 SDRAM devices. In the traditional implementation of this circuit the ASIC is packaged in it’s own high performance, thermally enhanced flip-chip BGA package. This package may have more than 1400 pins at 1.0 mm pitch. The memory devices are typically packaged in standard TSOP packages and mounted to the motherboard surrounding the ASIC device. In addition, some 100 passive components must be mounted to the motherboard to complete the subsystem schematic. This solution requires a significant amount of space on the motherboard. All of the signal integrity and timing issues associated with communication between the ASIC and memory must be managed on the motherboard by the system board designer. Finally, the routing complexity required drives up the complexity and cost of the motherboard.

Amkor has developed a solution whereby the ASIC device is mounted as normal in flip-chip configuration and the memory devices are mounted on the same substrate along side the ASIC. Decoupling capacitors and other passives can also be mounted to the substrate. Memory devices are packaged, tested and burned-in in individual FBGA packages before they are mounted to the substrate using a conventional surface mount process. This eliminates the yield loss issues associated with memory in traditional MCM designs. Since all routing between the ASIC and memory is done of the first or second layer of the ASIC package substrate rather than on the motherboard, signal delay is reduced. Integrating the ASIC and memory in a SiP format using a high-density substrate can result in significant cost savings by reducing routing complexity and layer count in the motherboard. Also, the SiP solution can save a significant amount of space on the motherboard, which will enable more functionality to be integrated in a system board. The SiP equates to a functional block of the system that can be standardized across a product family and dropped in to a new system board design with minimal effort.

When comparing the cost of an SiP solution to the cost of the same set of ICs packaged in individual packages, it is important to consider the total system cost. In some cases, an SiP package may be more expensive than the total package cost of the chips if they were packaged individually. However, the SiP solution usually results in system cost savings by reducing motherboard cost, reducing system size, and simplifying system assembly and rework processes. These factors should be taken into account when evaluating the cost of an SiP relative to other options.

Other High Speed Digital Applications
Another application of SiP technology is performance improvement of high-speed digital devices. As switching speeds increase and core voltages decrease the noise in the package can become a limiting factor for device performance. Traditional methods of handling signal integrity issues by placing passive components on the motherboard may no longer be adequate. The performance of standard wirebond PBGA packages can be improved by adding decoupling capacitors or termination resistors to the standard BGA package.
Decoupling capacitors placed between the power and ground ring in the package reduce ground bounce, resulting in a much lower bit error rate. The placement and value of the decoupling capacitors is critical. These components can be added to a standard BGA package using a standard surface mount process.

This capability to integrate SMD components in a standard semiconductor package also enables a designer to implement a given chip set plus all of the passive elements that complete the sub-system schematic in a single SiP-PBGA package. The result is lower system cost since a single, small SiP-PBGA replaces multiple discrete packages and passives mounted to the motherboard. It also improves system performance since most signal integrity issues can be managed within the package itself. This simplifies the job of the system board designer significantly. Typical applications of SiP-PBGAs include xDSL chip sets, DSP chip sets and graphics control modules.

We can take the power of integration that SiP-PBGA has to offer a step further by utilizing advanced interconnect technologies, such as stacked die in the SiP-PBGA format. Take for an example an xDSL chip set containing 4 die, 2 of which are identical, and some 10 passive components that complete the sub-system schematic. All of these components could be contained in a single 35 mm SiP-PBGA. If we now stack the 2 identical die on top of each other in the package, we can reduce the SiP-PBGA body size to 27 mm. Both size and cost of the SiP-PBGA are reduced and less space is occupied on the motherboard.

**SIP DESIGN FOR DIGITAL APPLICATIONS**

System-in-Package solutions tend to be more engineering intensive from a package design standpoint and they typically require cooperation between the IC manufacturer, package design and assembly subcontractor and OEM at the earliest stages of the design cycle. Failure to engage all of these parties early in the design cycle will result in imposing constraints that limit the ability to optimize cost, size and performance of the SiP and the system as a whole. System engineers, signal integrity engineers, layout specialists, silicon designers, testing and manufacturing teams have no choice but work together concurrently within an optimized design environment. The advance in computing, optics, and telecommunication industries brought numerous challenges to the signal integrity engineering community. The SiP designer is continuously challenged with miniaturization, cost reductions, and performance enhancements. High-density routing must be free of ringing, oscillation, overshoot, and undershoot, cross talk, settling time violations, and radiation.

The SiP design engineering team needs to be involved with the die design and I/O buffer distribution in the early stages of the design cycle. A simple change in I/O buffer locations on the die may lead to a re-design of the entire SiP. Detailed and thorough design and analysis is required within final system environment of the SiP. The analysis should take into consideration the SiPs interface with the motherboard and even daughter boards to satisfy OEM’s specifications.

**Initial Design Stage**

The initial design stage requires careful review of the system specifications and requirements. The SiP design engineer should follow the following procedures:

- Complete a project specification review of the schematics, BOM file, circuit netlist, signal descriptions, and timing diagrams. Thermal requirements and reliability requirements are also reviewed.
Substrate selection: The substrate has many attributes and properties that affect the design. Higher dielectric constant increases signal delay. The loss tangent must kept as low as possible (near zero). High loss tangent will lower signal detection sensitivity and increases the Bit Error Rate in the system. The substrate stack-up needs to be characterized for numerous impedance designs such as 50-Ohm single ended lines and 100-Ohm differential lines at the same layer within manufacturable design rules limitation. Top and bottom layer solder mask thickness impacts the impedance and capacitance of the signal paths. Via structure, line width and space design rules also affect circuit performance and signal routing density estimates.

Flip-chip vs. wirebonding: Wirebond has been used very successfully for many years, and it will continue to be used in future. A new generation of low voltage and high switching pattern applications may need to use flip-chip. Wirebonds tend to have larger DC voltage drop compared to flip-chip interconnects. The DC voltage path starts from a power plane and goes through the wirebonds to power pads on the die, and then from power pads to the middle of the die. This long path may not be acceptable for some low voltage applications (see Fig 2). Flip-chip bump distributions supply all the die segments with a minimum voltage drop. In addition the flip-chip interconnect technology reduces the inductive path for the signals. Flip-chip also can simplify the thermal solution in an SiP since it becomes easy to heatsink the die directly. However, flip-chip is still more expensive than wirebond in most cases, so the decision to use flip-chip is driven by either high interconnect density, thermal performance or electrical performance requirements. Note that the performance benefits of flip-chip are usually only realized if the device is designed for flip-chip interconnect. Die which are designed for wirebond and converted to flip-chip using a redistribution layer contain routing on the redistribution layer which in some cases is no better than wirebonding.

Passive components
Passive components are an essential part of many digital, mixed mode, and RF System-in-Package designs. Passive components used in SiP products can be categorized in to the following segments:

- RF application: Combination of inductors, capacitors and resistors in discrete or embedded format can be used for impedance matching, tank circuitry, tuning crystal oscillator, filters, discriminators, pre-emphasis, de-emphasis, transistor biasing and feedback circuitry.
- De-coupling capacitors are used to short power and ground planes at higher frequencies to eliminate and filter AC signal and to control power fluctuations on system power structure.
- By-pass capacitors are used to block DC voltage between two terminals and to control DC biasing at any node. For example, the input of a Low Noise Amplifier (LNA) may have a DC offset. To block this DC voltage from propagating to the antenna a bypass capacitor needs to be inserted between both blocks.
- Biasing resistors are used to bias transistors or to reduce DC level to a specific value.
- Pull up and pull down resistors depending on the voltages polarities improve the signal quality and eliminate oscillations on the unused receiver inputs such as an EIA standard RS-232-D serial port. The pull-up or pull-down resistors need to be at least 10X-30X greater than the driver output impedance to have negligible effect on the output impedance. The resistor values are very sensitive to other peripherals attached to the main system.
- Termination resistors and capacitors: Series termination and parallel AC terminations are two termination methods used universally to improve signal integrity of electronic systems. Both
termination techniques can be used for unidirectional and bi-directional bus systems.

Series termination resistors reduce the output buffer current and edge, which leads to reduction in signal ringing, reflections overshoot and undershoot with single and multi loads. The location of series resistor is design dependent. Most of the CMOS I/O buffers have less than 15-Ohm impedance of the transmission lines. Series resistor (ZSR) could be used to match the I/O buffer impedance (Zbuffer) to the characteristic impedance of the transmission lines on the substrate:

\[ Z_{\text{buffer}} + Z_{\text{SR}} = Z_0 \]

Small value (10-51 ohm) resistors are typical values for series termination resistors. In some cases series resistor is undesirable to be place at the buffer output, or signal timing is critical, then two parallel resistors termination used at the receiver end to dump unwanted signals.

Figure 8 illustrates parallel resistors termination techniques. RA consumes DC current when output is low. RB consumes DC current when output is high. Using both resistors (Thevenin equivalent) will reduce current consumption to half of the single termination cases.

AC termination uses pair of resistor and capacitor. The type of termination consumes no DC with the logic in either high or low states. 51-Ohm resistor and 10pF-68pF capacitor values are typical values used for AC termination.

- Diodes have numerous applications in electronic systems. Transient suppressor diodes are used to protect the silicon from ESD, and from power-off fault conditions. Clipping diodes are used to control unwanted oscillation or reflection signals. The diode is a necessary component for battery charge protections or to isolate the batteries from power supply when system powers on and off. One needs to carefully consider diode’s reverse voltage leakage current specification so as to not degrade battery life for portable appliances.

Power and thermal estimation:
Accurate wattage data is absolutely necessary to design the thermal path for heat dissipation. The effect of the system environment, package and die design on the SiP’s thermal performance needs to determined using 3D solid modeling, based on finite element simulations, to calculate:

- \( \Theta_\text{JA} \) for ranking package performance
- \( \Psi_\text{JB} \) for predicting package performance in system without heat sinks
- \( \Theta_\text{JC} \) for predicting package performance in a system with heat sinks

Die flag, thermal via distributions, power and ground planes’ copper thickness and power/ground ball assignment must be altered and optimized for the lowest cost thermal management solution.
Pre-Layout
Once package selection is completed the pre-layout stage can begin. Pre-layout design consists of the following 5 stages:

1. Read the netlist, die and die pad coordination into the design tool.
2. Identify all the electrical requirements and constraints for the design
3. Design controlled impedance for specific impedance value and differential lines using 2D or 3D parasitic extraction tools.
4. Input all the timing requirements and electrical constraints to the layout tool. The electrical constraints need to include noise budget, maximum threshold levels for overshoot, undershoot, ringing, reflections, and flight times.
5. EDA tool places the parts based on the given electrical requirements.

Final Design Flow
The next stage is to implement the final design flow:
1. Power and ground design: A typical design may include up to five different voltage potentials (3.3V, 2.8V, 2.4V, 1.8V and 1.4V). Careful consideration needs to be paid to the current return path for each segment of the design. Power and ground planes need to be portioned to accommodate different voltage levels. Both vertical (balls, vias, wires, bumps) impedance and horizontal (plane and trace) impedance needs to be optimized to reduce noise and voltage fluctuations.
2. Signal assignments to the ball grid array (BGA) or land grid array (LGA): Ball assignment is a key to optimize signal integrity performance. Grouping I/O signals is required to minimize cross coupling among different functions such as graphic, memory, and processor sections. The functional segments may need to be distributed on opposite sides of the package. Distributing enough power and ground balls is vital for package performance.
3. All the clock traces must be guarded and isolated from rest of the signal traces to minimize radiation EMI and SI problems during manual routing. Avoid routing clock traces under dies or across non-continuous power and ground planes.
4. Layout the design using time and electrical constraint driven auto routing tool based on the inputs from pre-layout stage. Designers may alter the design manually as needed.
5. Signal integrity and functional verification will follow as soon as the layout is done. Automated Signal integrity tools for comprehensive and thorough verification such as XTK-Quad, SpectraQuest-Cadence, ICX-Mentor Graphics, HyperLynx-Boardsim or other general purpose SI
tools can be used to speed up the analysis. Detailed analysis using spice simulator and full wave parasitic extraction tools may be necessary for a few traces such as clock or PLL traces.

6. All of the signal integrity issues regarding I/O signals need to be resolved. Termination resistors may be added to the SiP to improve signal quality as shown in figure 12.

7. Power distribution system design is becoming an increasingly difficult challenge for CMOS designers. CMOS geometry is shirking, operating DC voltage is decreasing to manage thermal dissipation, and transistor-switching speed is getting faster than ever. Simultaneous Switching Noise (SSN) can affect system performance and cause logic to switch state falsely, with a catastrophic failure to the system.

![Figure 12](image1.png)

**Fig 12.** Using passive components to improve the signal quality of the system

![Figure 13](image2.png)

**Fig 13.** De-cap capacitor effect on SSN reductions
SSN is the noise generated in high-speed components by simultaneously switching of multiple device outputs. The package is usually the biggest contributor to this noise, even though it is actually generated in all parts of the power distribution and interconnects between the system power supply and the integrated circuits. De-coupling capacitors are used extensively in the circuit design to solve signal integrity problems, which includes both SSN and EMI Problems. Usually, integrating decoupling capacitors in the package is more effective than placing them on the mother board.

SiP MANUFACTURING
From an assembly process standpoint, SiP is the convergence of state-of-the art IC assembly technology and surface mount assembly technology. It is the convergence of these assembly technologies that is both flexible and powerful. The ability of a company to be successful in SiP relates to how well they merge the IC and board level assembly technologies. Companies that want to participate in SiP primarily are either OEMs or EMS (Electronic Manufacturing Service) companies already expert at board level assembly or they are IDMs or package assembly companies already expert at IC assembly. Although it will be difficult for either type of company to assimilate a new technology to be able to manufacture SiPs, one can argue that IDMs and package assembly companies will have an advantage. This is because IC package assembly is generally more demanding than board level assembly – the interconnect pitches and bond pad sizes are an order of magnitude smaller, the reliability requirements are more stringent, the equipment and processes are more specialized to certain package types, and factory cleanliness levels are stricter (e.g. class 1000 vs. class 10,000 for board level assembly). SiP solutions are commonly extensions of standard IC packaging manufacturing platforms. For example, laminate-based RFPA modules can be based on standard FBGA manufacturing processes with the addition of surface mount equipment for integration of passives. Therefore, we would expect that companies familiar with IC package assembly will have a better ability to enter the SiP market, at least initially.

CONCLUSION
System-in-Package technology represents the convergence of advanced IC packaging technology and more conventional surface mount and mechanical assembly. SiP designers and assemblers must be able to draw from a broad technology portfolio including advanced IC packaging and surface mount assembly processes, test methods, materials and design tools and be able to combine these various technologies in order to optimize the packaging solution for each application. As a result of this capability to combine a broad portfolio of test technologies in various ways, the manifestation of SiP technology can take on seemingly limitless formats. Likewise, the application space for SiP is diverse. SiP design is also generally more engineering intensive than standard IC packaging. The SiP package designer must be involved early in the design cycle so that cost, size and performance of the SiP and the system can be truly optimized.