Introduction .................................................................................................................. ........................................................ 1
EMI Affect on System Design ................................................................................................... ................................................ 1
   Modes of EMI .................................................................................................................. ............................................... 1
      Differential Mode or Conducted Electromagnetic Fields ......................................................... 1
      Common mode or Radiated Electromagnetic Fields .............................................................. 1
   Convention Methods to Reduce EMI .............................................................................................. .................................... 2
Why Spread-Spectrum-Clock Generation? ......................................................................................... ........................................ 2
Addressing EMI Problems at the Source .............................................................................................................................  3
Selection Criteria of a SSCG for System Design ......................................................................................... ........................................ 3
   Meeting EMI Regulation Tests .............................................................................................................................  3
   Maintaining System Performance ......................................................................................................................  3
   Minimal Impact on Overall System BOM Cost ........................................................................................................  3
Trade-off Between Jitter and SSCG Effect .................................................................................................................................. 4
Why the Fujitsu SSCG? ......................................................................................................... .................................................. 4
   Digital Frequency Modulation Control Technique ........................................................................................................ 4
   Multi-Output Clock Products............................................................................................................................  5
   Programmability of SSCG ................................................................................................................................................ 6
      Optimization of Performance ......................................................................................................................... 7
      Impedance Matching ............................................................................................................................. 7
      Output Frequency and Modulation Control through Serial I/F .............................................................. 7
      SSCG’s Register Programming through I2C Interface ................................................................................. 8
      Programmability of Frequency Modulation .................................................................................................. 9
   Pin Compatibility and Package Options ................................................................................................. .................................... 9
   Low Voltage, Low Power Options ...................................................................................................................  9
Hardware Implementation and Guidelines for Board Design ........................................................................................................  9
   Spread Spectrum and Modulation Techniques ........................................................................................................ 10
      Center Spread vs. Down Spread ................................................................................................................... 10
      Modulation Carrier Frequency .................................................................................................................. 11
      EMI Reduction for Harmonics .................................................................................................................. 11
   SSCG and Data Transfer Using FIFO ................................................................................................................... 12
   Consideration of SSCG’s Modulated Output for Communication Systems ............................................................. 13
Application Examples ................................................................................................................. ................................................. 14
Conclusion..................................................................................................................... .....................................................  15
Introduction

Electromagnetic Interference (EMI) is a major challenge for designers of electronic devices. In the US, the Federal Communications Commission (FCC) tightly regulates the maximum amount of EMI that any electronic device may emit. The FCC regulations are designed to make sure that electronic devices will not interfere with each other (e.g., not losing TV reception while talking on your cordless or cell phone). EMI will be generated when the system is working based on frequency reference.

The technique, which involves modulating the reference frequency, is able to substantially reduce the amount of EMI created by the frequency reference and is often called “spread spectrum.” The Fujitsu Spread Spectrum Clock Generator (SSCG) family includes a variety of devices that modulate clock frequencies to attenuate peak emissions in computers, printers, MP3 players, cell phones, and other products that operate at increasingly higher frequencies. This application note introduces the Fujitsu SSCG, its key benefits and design guidelines and is intended to help system designers select a SSCG solution.

EMI Affect on System Design

As electronic products become faster and more complex, radiated-EMI emissions increase dramatically. With technology advances and increase of wireless connectivity features in portable products, the probability of interference between systems makes EMI a major concern.

During system development, critical signal-integrity and EMI simulations are difficult, time-consuming and error-prone due to their reliance on hard-to-predict models and parameter extractions. This situation worsens with every new product generation due to steadily increasing clock speeds and decreasing supply voltages. EMI on a low power supply voltage system is less than one with a high power supply voltage. Although simulating electronics systems to predict EMI levels is a difficult and time-consuming task, understanding the fundamental causes of electromagnetic radiation is very important.

Any charge moving in an electrical field or change in a field emits electromagnetic radiation. The strength of radiation is directly proportional to the rate of change. The sources of electromagnetic emissions can be intentional transmitters, such as cellular phones. But digital systems, such as PCs, PDAs, printers, and scanners, emit unintentional radiation. In digital systems, periodic clock signals are the major causes of EMI radiation. In addition, control and timing signals, address and data buses, interconnect cables, and connectors also contribute to EMI emissions.

Modes of EMI

There are two main modes of electromagnetic radiation:

• Differential mode or Conducted electromagnetic fields
• Common Mode or Radiated electromagnetic fields

Differential Mode or Conducted Electromagnetic Fields

These are a result of local current loops between PCB (printed-circuit-board)-interconnect traces and the ground planes. Using the conventional method, this type of noise is suppressed by installing a filter on the (VCC) side on the signal line or power supply line.

Common Mode or Radiated Electromagnetic Fields

These are a result of the coupling of ground and power-plane noise into traces, I/O buses and cable lines. With an AC power supply line, for example, noise is conducted on both lines in the same direction. With a signal cable, noise is conducted on all the lines in the cable in the same direction. Therefore, to suppress this type of noise, EMI suppression filters are generally used on the lines on which noise is conducted.
Another very common source of EMI is a high-frequency processor simultaneously accessing various addresses on a data bus. It can produce a lot of noise at multiple harmonics of the fundamental clock frequency. This type of noise can be both conducted and radiated.

SSCGs are especially effective for reducing such Common mode radiations.

**Conventional Methods to Reduce EMI**

As shown in Figure 1 and Figure 2, designers widely employ low pass filters to reduce EMI emissions that clock and timing signals generate. They reduce rise and fall times by filtering out higher-order harmonics. But this option might not be viable in high-speed systems because such filtering reduces the critical setup-and-hold-time margins and also signal overshoot and undershoot. A major problem with filtering rests on the fact that this technique is not systemic, meaning that reducing EMI emission at any given node in the system does not reduce the emissions in the other nodes. Because designers start with little information, they must provide filter placement in many suspicious locations, wasting valuable time and PCB space.

Shielding is a relatively simple way to reduce EMI emissions by containing them within the system and fully or partially covering the emission locations with grounded conductive shields. Shielding can be an effective approach in systems with strong emissions in which space, weight, and cost are unimportant. In most systems, however, especially portable and handheld products, shielding becomes the least desirable method of EMI reduction. Shielding increases the size, weight, and cost—creating a substantial increase in labor costs, for example, because the shielding of these products is difficult to automate in manufacturing.

Why Spread-Spectrum-Clock Generation?

A more effective and efficient approach is to use spread-spectrum-clock generation (SSCG) to control and reduce EMI emissions. Instead of maintaining a constant frequency, the SSCG technique modulates the system-clock frequency with a much smaller frequency—typically 10 to 50 kHz—to control and reduce EMI emissions at their source, the system clock. The systemic nature of SSCG has a major advantage over other EMI-reduction techniques because all clock and timing signals derived from the spread-spectrum clock are also modulated at the same percentage, leading to a dramatic EMI reduction throughout the system.

The effect of EMI decrease is shown in Figure 3 on the next page with the ratio of the electric power indicated with the decibel mark when the modulation is On/Off. This is represented in following formula:

\[ 10 \times \log_{10}(P_1/P_2) \]

Where \( P_1/P_2 \) is Electric field strength at modulation functions On or Off.

1. EMI decrease effect = 0dB when modulation is off
2. EMI decreases effect = -6dB when \( P_1/P_2= 1/4 \)
3. EMI decreases effect = -20dB when \( P_1/P_2= 1/100 \)

SSCG can reduce the radiated emissions of the digital-clock and timing signals. One can achieve EMI reduction by frequency-modulating the system clock with a low-frequency signal. This approach creates a frequency spectrum with sideband harmonics. Intentionally broad banding the narrowband repetitive system clock simultaneously reduces the peak spectral energy in both the fundamental and the harmonic frequencies.
The SSCG technique is analogous to the spread-spectrum technique in communications applications. However, it does not spread encoded information over a wide bandwidth, as CDMA (code-division multiple access) does, and the only benefit of using SSCG is to reduce undesired EMI emissions.

**Addressing EMI Problems at the Source**

A fundamental EMC design principle requires that EMI be attenuated at its source on the PCB. Spread-spectrum techniques are methods by which energy generated in a particular bandwidth is deliberately spread in the frequency domain, resulting in a signal with a wider bandwidth. A spread spectrum clock generator (SSCG) performs this spreading for designers.

**Selection Criteria of a SSCG for System Design**

When selecting a spread spectrum clock to attenuate EMI for a consumer product, developers must ensure following factors:

**Meeting EMI Regulation Tests**

Agencies, such as the Federal Communications Commission (FCC), regulate the amount of radiated energy in terms of voltage, distance and frequency. The FCC has two classes of radiation levels, stated as Class A and Class B. Class A devices are digital devices intended for use in commercial, industrial or businesses and not intended for use by the general public or in the home. Class B digital devices are intended to be used in the home but could also be used elsewhere. In general, Class B levels are more difficult to meet than Class A. Hence a good frequency profile and modulation frequency are the most important factors when choosing a SSCG product. A high-quality frequency profile gives the best performance in EMI reduction—a triangle frequency profile requires a larger spread amount to achieve the same EMI reduction. Higher modulation frequency usually offers higher EMI attenuation.

**Maintaining System Performance**

First, the Phase Lock Loop (PLL) must run at an optimum state, i.e., high VCO frequency, appropriate bandwidth, etc. Second, the frequency spread amount usually should be as small as possible to keep system the timing margin high and the cycle-jitter low. For down spread, a lower spread amount makes a system run less slow by not reducing too much on average frequency. The frequency spread method should be chosen based on application.

**Minimal Impact on Overall System BOM Cost**

Use of a SSCG can result in a significant reduction of system radiated EMI. This can result in dramatic cost savings for the system by using multi-clock and programmable SSCG products that could be estimated in the range from less than $1 to $10 or more if integrated with an ASIC or other special features.

Conventional techniques for reducing EMI include shielding ground planes, adding filtering components and providing additional shielding. Going from a two-layer board to a four-layer board to insert additional ground planes could easily cost about $5–6. Filtering EMI typically uses ~$0.25 worth of resistors, inductors, and capacitors, and often $0.70 worth of common mode chokes and toroids. In many cases filtering will not be enough to allow a system to pass EMI tests, in which case costly shielding may be required. Shielding can easily add several dollars to the cost of a system.

For example, if even one requirement is not met, no matter if it is EMI or jitter performance, applications are more likely to require a modification to the system clock. Hence the flexibility of a programmable EMI approach offers insurance by reducing potential development cost and risk. Fujitsu SSCG products can add value in this regard.
Trade-off Between Jitter and SSCG Effect

A SSCG may not always be the perfect answer for all applications and systems. It has little effect, for example, when used in places where differential mode noise is being generated. Differential mode noise is best addressed with conventional components like decoupling capacitors and ferrite beads. Copiers, for example, use a large number of AC motors. When AC motors are driven, they emit showers of tiny sparks, and the electromagnetic waves generated by these sparks are differential mode noise. A SSCG has less impact on differential mode noise.

There is a trade-off between cycle to cycle jitter and the SSCG effect. The key points come into play when using a SSCG to lower the frequency spectrum peak while controlling jitter: degree of modulation and modulation waveform. Hence SSCG products have been made programmable for parameters like degree of modulation and waveform cycle etc. SSCG’s effectiveness increases as the degree of modulation rises, because this lowers the clock signal frequency spectrum peak. At the same time, though, jitter and variation between signals rise. The reduction in the frequency spectrum peak is dependent on the waveform. Standard waveforms have steep angles close to the peak values (the peaks and troughs in the waveform), and the frequency spectrum spread effect is greatest on waveforms which are smallest at the zero-cross point. Fujitsu SSCG products feature program parameters like degree of modulation and waveform cycle to meet this trade-off.

Why the Fujitsu SSCG?

The Fujitsu SSCG family includes a variety of devices that modulate clock frequencies to attenuate peak emissions in computers, printers, MP3 players, DVD players, cell phones, and other portable products that operate at increasingly higher frequencies. Peak radiation noise is reduced by slightly modulating oscillation frequencies with the internal modulator.

A SSCG can suppress the peak of unwanted radiation by modulating the frequency. It is effective for not only the oscillation frequency of clock (basic wave) but also of the higher harmonic wave.

Following are technology strengths of Fujitsu SSCG products.

Digital Frequency Modulation Control Technique

The Fujitsu proprietary technology is based on current control method, which is unlike other methods available on the market such as Compensated voltage control and Frequency control methods.

Using conventional frequency modulation, an analog control technique, is insufficient at EMI reduction due to the formation of a peak in the diffused spectrum.

Current control method is shown in Figure 4.

![Figure 4 - Current Control Method](image)

Figure 4 – Current Control Method

![Figure 5 - Ideal Modulated Waveform](image)

Figure 5 – Ideal Modulated Waveform
An ideal modulated waveform can be generated with digital control by using a current D/A converter (IDAC) resulting in a reduction of about 19dB (Modulate ±1.5%) of EMI as shown in Figure 5 on the previous page. The influence on cycle to cycle jitter is also small. An accurate modulation can be achieved by the current control method.

A complex multi-cycle modulation waveform further increases the performance of Fujitsu’s spread spectrum clock generators. Unlike modulation at single cycle, Fujitsu’s multi-cycle modulation reduces the peak by distributing it by the compound modulation method, which enables more flat spectrum diffusion. Thus, effectively about 19dB can be achieved (at modulation depth ±1.5%) as shown in Figure 6.

The repetition rate is device and configuration dependent. For example it may sweep between 2000 and 2600 input clock periods. Due to digital modulation using current control method, power consumption is minimum.

Fujitsu technology thus helps in system design for:

- Effectively decrease EMI
- Low cycle to cycle jitter (less than 100ps-rms at no load capacitance and standard deviation)
- Low power consumption (e.g. MB88182 at 1.8V when all clock outputs are active consumes 0.5mA; when all clock outputs are disabled it consumes 1uA)

**Multi-Output Clock Products**

The Fujitsu SSCG MB8818x series has devices with multi-clock outputs. Multiple-PLL and multi-output SSCG products with selective use of spread-spectrum-clock functions enable users to integrate many functions, such as buffers and level translators. Using multiple, unique programmable-frequency outputs in the same product eliminates a large number of crystals and crystal oscillators by using a single-standard, first-order crystal, saving additional cost and PCB space as shown below in Figure 7.
Programmability of SSCG

For end-customer system design, if none of the spread percentages satisfies the system, developers must request the clock manufacturer to make design changes and manufacture a new chip, which at best takes several weeks even for a simple metal layer change and is often very expensive.

Alternatively, the Fujitsu programmable spread spectrum clock generator MB88182 series provides general purpose clocks supporting field programmability of registers. MB88182 block diagram is shown in Figure 8.

Roadmap products like the MB88R157 series that are currently under development have the combined features of programmability and on-chip non-volatile memory like Ferroelectric RAM (FRAM). FRAM enables dynamic reconfiguration of spread parameters, eliminating slow and expensive chip design changes. Embedded FRAM, an industry first, features fast rewriting speed and can vary its frequency output over a range of 1- to 134MHz while mounted on a circuit board. Such products are appropriate for a wide range of applications including multi-functional printers, PCs, and mobile phones, as well as for televisions, DVD players, and game consoles.

While selecting SSCG products, there are important factors to consider that offer flexibility in the customer’s system design and help reduce system BOM cost. Factors listed below are also described in Table 1 on the next page.

- Programmable parameters and their range/resolution such as:
  - Output frequency range
  - Low output skew
  - Output drive strength
  - Rise and fall times of output
  - Duty Cycle
  - Spread Spectrum Modulation range (in kHz) and techniques
  - Spread Spectrum ON or OFF options
- Low power supply: 1.8V, 2.7V and 3.3V power supply operation options
- On chip oscillator and its resolution
- Low power dissipation
- Low cycle to cycle jitter
- On chip non-volatile memory for storing programmable parameters
- Serial communication interface like I2C options for system interface in case of no on-chip memory
- Data transfer methods and techniques
- Multi-clock output options to reduce system BOM cost
- Low cost, compact package options
- Pin or footprint compatibility of products to reduce design cycle time on customer’s platform

![Figure 8 – Programmable, Multi-clock Output SSCG MB88182 with I2C](image-url)
Optimization of Performance
The advantage of using Fujitsu programmable SSCG products is that it improves and optimizes various timing specifications and parameters within the system-timing budget.

Programmability also allows optimization for the best spread spectrum clock performance at desired specifications as per customer requirements.

Programmable parameters and ranges for the Fujitsu SSCG are described in Table 1. The programming GUI tool of the MB88182 is shown in Figure 9 on the next page as an example that allows users to configure parameters mentioned in Table 1. This product has multiple PLLs and multi-clock output features. It has 3 outputs for the built-in PLL (one output with just PLL and 2 outputs with the Spread function with PLL) and 2 outputs of Spread function and a Reference clock.

Impedance Matching
One of the most critical considerations of clock-signal integrity is the matching of the impedance of the board trace and driven load to the clock driver. This matching ensures that the clock signal is free from overshooting or undershooting and ringing for each of the driven clock signals. Programmable clocks achieve this goal by providing adjustable impedance levels at each clock-output driver to ensure a good match to various load-impedance levels.

Output Frequency and Modulation Control through Serial I/F
Frequency margining is possible with programmability. Margining is the stepping up or down of output frequency through frequency-control pins or through the I2C serial interface that could easily configure register settings of the SSCG device. The technique is both useful and easy to implement under automated-testing systems to find potential system weaknesses and failures during the product-development and production phases.

The fine, gradual increase or decrease of the system-clock frequency sweeps the range of the frequency to detect any irregularities or failures for a given frequency range. It is easily implemented using programmable clocks by setting both center- and extreme-frequency limits for changing system requirements. In addition, one can test the margin of other critical timing parameters, such as clock skew, spread amplitude (percentage), or spread-modulation rates to verify that the receiving PLL in an ASIC or other system-component interface has sufficient built-in bandwidth and timing margins.
Following methods explain set up of programmable SSCG devices.

SSCG’s Register Programming through I²C Interface, e.g the Fujitsu MB88182
Some programmable SSCG devices like the MB88182 do not have embedded memory to store the configuration of spread spectrum parameters. In such cases, any system processor or MCU with embedded FLASH memory can communicate with the SSCG through the I²C interface. In such a scenario, the MCU’s I²C acts as master to send programmable parameters to the slave SSCG device registers. The Fujitsu’s SSCG programming tool allows the user to configure the PLL or output frequency value, and several parameters are listed in Table 1. Figure 9 lists such a setup example for the I²C interface. The programming tool generates a text file format with register values that can be programmed into the SSCG MB88182 through the I²C. The MCU’s initialization and I²C protocol source code samples are available through Fujitsu Microelectronics.

SSCG Programming Tool for Product with On Chip Memory-Example For MB88R157 (Under Development)
Figure 10 shows the programming set up of the SSCG device with on chip memory.

A special Fujitsu BGM (Background Monitor Debug) adapter is used in between the PC and the SSCG. Fujitsu’s SSCG programming tool installed on the PC allows the user to configure the PLL or output frequency value and several parameters as listed in Table 1 for the MB88R157. The Fujitsu BGM adapter interfaced with the SSCG board programs the device for user-configured parameters.

Table 2 shows cable connections (10 pins) between the BGM adapter P1 and the SSCG board connector P2.

<table>
<thead>
<tr>
<th>P1: Connector pin #</th>
<th>Name</th>
<th>Connection to MB88R157</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Open</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Connect to VSS terminal</td>
</tr>
<tr>
<td>3</td>
<td>BRSTX</td>
<td>Open</td>
</tr>
<tr>
<td>4</td>
<td>BDBMX</td>
<td>Open</td>
</tr>
<tr>
<td>5</td>
<td>BSOUT</td>
<td>Connect to OE terminal</td>
</tr>
<tr>
<td>6</td>
<td>BEXCK</td>
<td>Open</td>
</tr>
<tr>
<td>7</td>
<td>BSIN</td>
<td>Connect to OE terminal</td>
</tr>
<tr>
<td>8</td>
<td>N.C</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Connect to VSS terminal</td>
</tr>
<tr>
<td>10</td>
<td>N.C</td>
<td>-</td>
</tr>
</tbody>
</table>

Figure 10 – Programing Set Up with On Chip Memory

Table-2 Connection Between BGM Adaptor and the SSCG
Programmability of Frequency Modulation
Programmable clocks are also beneficial during EMC (electromagnetic-compatibility) testing because one can easily set frequency modulation to several values. Examples range between OFF, ±0.25%, ±0.50%, ±0.75%, ±1.00%, ±1.25%, ±1.50%, ±1.75%, ±2.0% based on product part number.

Such programmable attributes of the SSCG simplifies compatibility measurements during design and testing, eliminates product-introduction delays, and improves time to market. The second benefit of the SSCG is reducing EMI without degrading the timing-signal quality. The system references setup-and-hold times only to the rising edge of the timing signal. Because the rise and fall time changes by only the amount of the spread percentage when using a spread-spectrum approach, the process maintains the critical setup-and-hold-timing margins. Fujitsu SSCG products are integrated with additional programmable EMI-reduction and timing functions to further enhance system performance and reduce costs.

Pin Compatibility and Package Options
Some Fujitsu SSCG products are pin compatible to competitor products in the market. Some examples are the Cypress CY2581x series and W180 series and the Renesas HD151 Series; ICS170 and ICS 580 Series. Pin compatibility helps customers reduce the probability of redesigning the PCB and reduce resource and time for customer-system design. The MB88150 series devices are pin compatible with package options such as SOP8 (5.05mmx3.9mm). Fujitsu is a pioneer in packaging technology and has several package options such as TSSOP, SOP and fine pitch-compact BCC, packages.

Low Voltage, Low Power Options
Different output voltage options are supported by a single device - 1.8V±0.15V and 2.6V±0.1V. There is also a device lineup supporting 3.0V, 2.7V and 1.8V, which makes it suitable for portable consumer applications. All Fujitsu SSCG products have a power-down mode feature that reduces power consumption to a minimum. One example is the MB88182 device, which consumes only 0.01mW at 1.8V during the power-down mode of all outputs compared to the active mode at 0.9mW.

Hardware Implementation and Guidelines for Board Design

Figure 11 on the next page shows a circuit design example using the MB88154.

Based on this example, guidelines for circuit design and PCB layout are listed below and shown in Figure 12 on the following page.

- It is recommended to connect in parallel electrolytic capacitors (aprox. 10μF) and ceramic capacitors (aprox. 0.01μF) between VSS and GND near the SSCG. The 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

- Noise near the XIN and XOUT pin may cause malfunction of the device. Design of the PCB should be such that traces of XIN and XOUT and other signals should not intersect.

- Traces from CLKOUT and REFOUT should be laid out as small as possible.

- No vias should be used between the decoupling capacitor and the VDD pin.

- The PCB trace to the VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

- An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the SSCG. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.
Spread Spectra and Modulation Techniques

Spread-spectrum clock generation is used in some synchronous digital systems, especially those containing microprocessors in embedded systems, to reduce the spectral density of the EMI that these systems generate. A synchronous digital system is one that is driven by a clock signal and because of its periodic nature, has an unavoidably narrow frequency spectrum. In fact, a perfect clock signal would have all its energy concentrated at a single frequency and as well as its harmonics, and would therefore radiate energy with an infinite spectral density. Practical synchronous digital systems radiate electromagnetic energy on a number of narrow bands spread on the clock frequency and its harmonics, resulting in a frequency spectrum that, at certain frequencies, can exceed the regulatory limits for electromagnetic interference (e.g. those of the FCC in the United States, JEITA in Japan and the IEC in Europe).

Spread spectrum clock oscillators spread out the concentrated mode energy on one particular frequency to a broader bandwidth and controlled frequency range with a controlled modulation rate.

There are two kinds of widely used modulation techniques: “Center spread” and “Down spread”. Choice is based on application.

**Center Spread vs. Down Spread**

The controlled modulation process can be on all of one side of the nominal frequency (down spread) or 50% up and 50% down (center spread) as shown in Figure 13.

For example if we pick 100 MHz SSCG, then its center frequency is modulated between 99.500 MHz and 100.500 MHz with the center spread at 0.5%; the frequency range is between 99.500 MHz and 100.0 MHz if the down spread is at 0.5%. By moving the center frequency, a down spread of 0.5% modulation can be considered a process equivalent to a center spread of 0.25%. In other words, modulation between 99.500 MHz and 100.0 MHz (down 0.5%) is equivalent to a center spread of 0.25% with a center frequency at 99.750 MHz, see Table 3.

The amount of EMI reduction is directly related to the depth of modulation of the reference frequency. Typical modulations are ±0.5%, or ±1%. The greater the modulation, the greater the EMI reduction. For example, for a 100-MHz reference signal, with a ±0.5% modulation, the reference frequency is swept between 99.5 MHz and 100.5 MHz.

When center modulation (±) is used, the system processing performance of a CPU will be the same as for a CPU using a non-modulated clock. Some system designers are concerned

<table>
<thead>
<tr>
<th>Table 3 – Center Versus Down Spread</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency Minimum</strong></td>
</tr>
<tr>
<td>100 MHz at center spread 0.5%</td>
</tr>
<tr>
<td>100 MHz at down spread 0.5%</td>
</tr>
</tbody>
</table>

Note: the above is equivalent to 99.750 MHz at center spread of 0.25%

**Figure 13 and 14 – Center spread and Down Spread**
about over boosting processors; if you use a processor designed for a 100-MHz reference, and that reference spends a substantial part of its time at 100.5 MHz, the processor may be operating at a higher than rated speed during that period of time.

To address this concern, modulation can be specified as “down only,” e.g., –0.5%. Such –0.5% modulation, in the same 100-MHz example, would only vary from 99.5 to 100 MHz. This is achieved by moving the center frequency down. The specified value of “100 MHz, with –0.5% modulation” could really be thought of as “99.75 MHz with ±0.25% modulation”. Using down spread only will result in some small performance degradation of a CPU, as the nominal 100-MHz signal is now something less than that.

**Modulation Carrier Frequency**

The modulation carrier frequency (sweep rate) is typically around the KHz range which is relatively slower compared with the MHz range of the clock frequency. As shown in Figure 15 on the following page, the output frequency is slowly swept within the pseudo triangle shape wave envelope from the f(max) to f0(nominal); then to f(min); then to f0(nominal); and back and forth. The time that is required to transition between f(min) and f(max) and back to f(min) is called the modulation rate TMOD. The resultant instantaneous frequencies are always between f(max) and f(min).

The modulation rates of spread spectrum clock generators are generally referred to in terms of frequency, and fMOD = 1/TMOD

The input clock frequency (fIN) and the internal divider determine the modulation rate as below:

\[ f_{MOD} = \frac{f_{IN}}{DR} \]

where:

- \( f_{MOD} \) is the modulation rate,
- \( f_{IN} \) is the input frequency,
- \( DR \) is the divider ratio.

The modulation percentage determines the bandwidth of the span while the modulation carrier frequency determines the spacing of the spectral.

Fujitsu SSCG products have option-in hardware for setting the modulation rate function as either as OFF or ON with different modulation rate settings for ease-of-use. Table 4 refers to such an example. The MB88162 has S0/S1 pins for the modulation setting function as shown in Table 4.

Table 4 – S0/S1 Modulation Rate Setting

<table>
<thead>
<tr>
<th>S1</th>
<th>S0</th>
<th>Modulation Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>At down spread</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>-1.0%</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>-2.0%</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>-4.0%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Modulation Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>At center spread</td>
<td>No Modulation</td>
</tr>
<tr>
<td>±0.5%</td>
<td>±1.0%</td>
</tr>
<tr>
<td>±2.0%</td>
<td></td>
</tr>
</tbody>
</table>

**EMI Reduction for Harmonics**

As shown in Figure 15, higher order harmonic frequencies do get stronger EMI reduction. They also show that the greater the modulation percentage the larger the reduction of EMI emissions. It needs to be pointed out that the fundamental frequency as well as every harmonic gets EMI reduction by spread-spectrum technology.
SSCG and Data Transfer Using FIFO

A very common source of EMI is a high-frequency processor simultaneously accessing various addresses on a data bus. It can produce a lot of noise at multiple harmonics of the fundamental clock frequency. This type of noise can be both conducted and radiated. The Spread Spectrum clock by itself cannot be used for asynchronous data communication. In such cases, a SSCG can be used along with a FIFO or Line Buffers. The SSCG output clock being asynchronous to the input clock requires systems that use data transfer to synchronize using a FIFO and other design techniques.

In electronics, there are two kinds of buffers: 1) buffer amplifiers that are used to stop noise transmitted from the output side to the input side, and 2) buffer memory that is used to temporarily store transfer data. “Buffer” used here refers to this buffer memory.

A buffer is used when data is input in variable amounts and at variable intervals, is output at a fixed interval and in fixed amounts, and when data is input at a fixed interval and in fixed amounts, and is output at random intervals. By using a buffer, data can be transferred smoothly between devices with different transfer rates.

Buffers usually use a FIFO system and are configured in steps as a ring structure. The size of the buffer is determined by the I/O speed differential and timing of the data being handled.

Following are example design guidelines for a FIFO system and a SSCG in 3 different scenarios of input and output clocks cases as shown in Figure 16 on the next page.

**Input Frequency = Output Frequency (1-fclk)**

It is possible for asynchronous communication to use a FIFO circuit and it is recommended to use a center-spread-spectrum clock. Asynchronous transfer is possible with using a FIFO with central spread SS clock, etc.

Estimation of the FIFO steps in this case:

FIFO steps depend on modulation rates as shown in below formula:

\[
\text{FIFO steps} = \text{ROUNDUP}(\frac{N_{\text{max}}}{2})(\text{modulation rate} / 2)^*2 + 2
\]

(“ROUNDUP” is round-up of digit)

The Fujitsu SSCG part numbers and their corresponding inputs, modulated output clocks and FIFO steps are given Table 5.

---

Table 5 – Fujitsu SSCG Part Numbers and Their Corresponding Inputs, Modulated Output Clock and FIFO Steps

<table>
<thead>
<tr>
<th>Part number</th>
<th>Suffix number / Function setting</th>
<th>Input Frequency</th>
<th>Max input clock number per modulation period. [Nmax]</th>
<th>FIFO steps each of modulation rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB88151A</td>
<td>100</td>
<td>16.6-33.4MHz</td>
<td>2200</td>
<td>±0.5% 8 8 20</td>
</tr>
<tr>
<td>MB88152A</td>
<td>110</td>
<td>16.6-33.4MHz</td>
<td>2640</td>
<td>±1.0% 10 14 22</td>
</tr>
<tr>
<td>MB88153A</td>
<td>110</td>
<td>33.0-67.0MHz</td>
<td>4400</td>
<td>±1.5% 14 22 22</td>
</tr>
<tr>
<td>MB88154A</td>
<td>112</td>
<td>40.0-80.0MHz</td>
<td>5280</td>
<td>±1.0% 16 42 42</td>
</tr>
<tr>
<td>MB88155</td>
<td>110</td>
<td>67.0-134MHz</td>
<td>8800</td>
<td>±1.5% 24 68 68</td>
</tr>
<tr>
<td>MB88155</td>
<td>112</td>
<td>16.6-40.0MHz</td>
<td>2640</td>
<td>±0.5% 10 12 22</td>
</tr>
<tr>
<td>MB88155</td>
<td>111</td>
<td>33.0-67.0MHz</td>
<td>4400</td>
<td>±1.0% 14 22 22</td>
</tr>
<tr>
<td>MB88155</td>
<td>110</td>
<td>40.0-80.0MHz</td>
<td>5280</td>
<td>±1.5% 16 42 42</td>
</tr>
<tr>
<td>MB88155</td>
<td>112</td>
<td>67.0-134MHz</td>
<td>8800</td>
<td>±1.5% 24 68 68</td>
</tr>
<tr>
<td>MB88155</td>
<td>113</td>
<td>12.5-25.0MHz</td>
<td>8800</td>
<td>±0.5% 6 8 8</td>
</tr>
<tr>
<td>MB88155</td>
<td>113</td>
<td>25.0-50.0MHz</td>
<td>1760</td>
<td>±1.0% 8 12 12</td>
</tr>
</tbody>
</table>
Input Frequency > Output Frequency
(1-FOCLK, Down Spread Spectrum Type)
It is possible for asynchronous communication to use memory or a FIFO that is sufficient to save the amount of transfer data. Asynchronous transfer is possible with enough memory / FIFO which stores the forwarding data when down spread SS clock is used.

Input Frequency < Output Frequency
(Minimum frequency of Spread spectrum Clock Output)
It is recommended just to use FIFO circuit. Asynchronous transfer is possible with a FIFO when the minimum frequency of the SS clock is high (input frequency<output frequency • (1 +/- modulation depth) compared with the input frequency.

Consideration of SSCG’s Modulated Output for Communication Systems
There are some systems that do not use the spread spectrum clock system directly. For example, USB and CAN are defined by a severe jitter standard. In the case of using SSCG in such systems, the spread spectrum clock modulation rate is only spread in the range of the defined standard. Also, it is obvious that the jitter specification of the clock receiver device is severe in such cases. Hence it is not a recommended practice to use SSCG’s modulated clock output directly for serial communication functions such as USB and CAN as they require a smaller budget for the phase error of the clock signal.

Figure 16 - Design Guidelines for a FIFO System and a SSCG
a) Instead, reference clock (also called non-modulated clock) output from the REFOUT pin of the Fujitsu SSCG (as shown in Figure 8) can be used in such cases as shown in Figure 17.

b) In the case of a printer application, it is recommended to supply the reference clock (from the REFOUT pin) to the IO controller and the modulated clock to the rest as shown in Figure 18.

c) When a SSCG is used for a MP3 player application, it is recommended to supply the reference clock to the USB and audio output and modulation clock to the rest as shown in Figure 19.

d) When a SSCG is used for a mobile camera or any image processing application (Figure 20), the reference clock should be supplied to the Encoder and Decoder blocks and the modulated clock output to the image processor. If the modulated clock is used for Encoder and Decoder functions, flicker noise may be observed in the product image.

**Application Examples**

Following applications have potential requirements for SSCG for system design:

- Printers & MFP
- Digital copiers
- PC/Netbook
- LCD monitors
- HDTV
- Portable navigation devices
- Storage devices
- Routers & servers
- Ethernet appliances
- LAN switches & hubs
- Digital embedded systems

Fujitsu SSCGs with multi-clock output and programmable products help reduce system BOM cost.
Conclusion

Spread-spectrum clocking has become more popular in portable electronics devices because of faster clock speeds and the increasing integration of high-resolution LCD displays for user interfaces. Because these portable electronic devices are designed to be lightweight and inexpensive, passive EMI reduction measures such as capacitors, ferrite beads or metal shielding are not viable options. Active EMI reduction techniques such as spread-spectrum clocking are necessary in these cases, but can also create challenges for designers. The main challenges among these are the risks associated with modifying the system clock which in turn has associated risks of clock/data transfer and modulation techniques as explained in this document. Suitable product selection and system design are critical.

Fujitsu SSCG products provide value to customer system design. Multiple-PLL and multi-clock output SSCG products with selective use of spread spectrum clock functions enable users to integrate many functions, such as buffers and level translators. Using multiple unique programmable frequency outputs in the same product eliminates a large number of crystals and crystal oscillators save additional BOM cost and PCB space. In systems already meeting EMC requirements, Fujitsu SSCG products could further reduce the emission levels to help reduce the total number of PCB layers and external component cost to contribute for overall system cost reduction and offer greater system design flexibility.