Multiphase buck converter design responds well to transients

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High current multiphase buck converters are finding use in computing, graphics, and telecom applications. Some careful design considerations, procedures and component selection will lead to successful multiphase converter designs in a variety of systems.

While allowing ever-higher levels of system performance, the trend toward smaller CMOS geometries and high packing density trend poses a serious challenge to the Power Supply designer. First, the smaller feature size requires a lower supply voltage to avoid avalanche breakdown. 1.5V to 1.8V is common today with sub 1V on the horizon. But the increasing number of transistors has caused current demands to grow significantly. Today, a single digital IC can require 20 to 50 Amps and as much as 200 Amps in the future. Even though voltage is dropping, the overall power required (Volts x Amps) is increasing from today's 30 to 50 Watts to 200 Watts within the next several years. To reduce power dissipation, it is common to start and stop operation during periods of inactivity. This leads to extremely high load current transient demands on the power supply. It must be able transition between zero and full load with slew rates of 30 to 50 Amps per microsecond today, increasing to 300 Amps per microsecond in the future.

The Multiphase Buck converter has recently emerged as the leading candidate for meeting the power challenge of the next-gen processor 1 and 2. This topology is depicted in figure 1 and consists of multiple synchronous buck converters configured to share current while powering a common load. The switching frequency of the converters is phase shifted resulting in cancellation of the ripple currents seen by the input and output filters.

Figure 1 - Multiphase Buck Converter
The advantage of the Multiphase Buck topology is that it is relatively simple and provides excellent transient response, high efficiency, small size, and low cost. The effective switching frequency is multiplied by the number of phases while the load is divided by the number of phases. The Multiphase Buck Converter is commonly powered from a 5V or 12V bus derived from an AC-DC power supply. The trend is towards using 12V to lower the bus current and therefore reduce resistive losses in the Printed Circuit Board (PCB) and connectors.

MULTIPHASE BUCK DESIGN CONSIDERATIONS

In order to generate a solution optimized for a particular application, the designer must consider a number of criteria. The final design approach can be determined after considering all of them and the resulting tradeoffs;

Number of Phases

The first thing to be considered is the optimum number of phases. Although increasing the number of phases reduces the ripple current in the input and output filters and potentially improves transient response, it also increases complexity, PCB layout difficulty, and at some point, cost. Usually, the choice is based on how many Power MOSFETs are required to efficiently handle the per phase output current. It is common to parallel MOSFETs to reduce the effective RDSon and reduce thermal impedance, especially for the synchronous rectifier. However, once it has been determined that four or more MOSFETs are required to handle the current in each phase, one should consider increasing the number of phases. This requires an additional output inductor but the increased cost and PCB area of these component tends to be offset by reductions in the cost and size of the input filter and output capacitors.

Current Per Phase

The performance of the MOSFETs tends to determine the optimal current per phase, which today ranges from 10 to 25A. Designs operating at lower switching frequencies, using state-of-the-art MOSFETs, and having low thermal impedance (heatsinks) tend to be in the upper end of this range.
Designs targeting compact size, maximum efficiency, fast transient response, higher switching frequencies, or use of mature lower cost MOSFETs tend to be in the lower end of the range. As future generations of MOSFETs become available, it will be possible to increase the current per phase without compromising efficiency or thermal performance. Switching Frequency

Higher switching frequencies tend to reduce the size and cost of the input and output filter, but lead to increased losses in the MOSFET switch. Non-overlap time between the conduction of the switch and synchronous rectifier MOSFET must be provided to avoid shoot-through of current from input to ground. This usually results in non-synchronous operation and efficiency reducing conduction of the synchronous rectifier body diode during each switch transition. Increasing the switching frequency tends to increase this loss as well. Another problem is that commonly used low cost inductors and capacitors have parasitic losses that increase with frequency forcing use of more expensive alternatives. Also, radiated and conducted EMI tend to increase with switching frequency. Finally, higher switching frequencies place additional burden on the PWM controller. With the components available today, the optimal per phase switching frequency for most multiphase designs is in the range of 150 to 400kHz. The optimal switching frequency can be expected to increase over the next several years, as improved components become available.

Transient Response

The value of the output inductor and the number of phases place a theoretical limit on the ability of the multiphase converter to slew its output current. This is due to the fact that the rate of the change of current in an inductor is equal to the voltage placed across it divided by the value of its inductance. The minimum response time to a load decrease can be calculated as follows;

\[ T_{MIN} = L \times \frac{IMAX - IMIN}{Vout} \] (1)

Likewise, the minimum response time to a load increase can be calculated by;

\[ T_{MIN} = L \times \frac{IMAX - IMIN}{Vin - Vout} \] (2)

The theoretical minimum response time is determined by the slew rate of each inductor divided by the number of phases. This time is further increased by the response time of the PWM controller and MOSFETs.

Unfortunately, the load current slew rate is often much greater than can be supplied through the output inductors. Therefore, it becomes necessary to add significant amounts of bulk capacitance at the output to supply current to the load while the inductor current ramps. Their parasitic resistance and inductance, as well as the impedance of the path to the load limit the effectiveness of the bulk capacitance. It is common to use a number of capacitors of different types in parallel to reduce the total parasitic impedance.

The change in output voltage due to a load step can be calculated as follows;
delta-Vo = delta-Io x (ESL/delta-It) + ESR + (TR/Co) (3)

Where: delta-Io is the change in load current, ESL is the Equivalent Series Inductance, delta-It is the load current slew rate, ESR is the Equivalent Series Resistance, TR is the regulator response time and is equal to equations (1) and (2) plus the PWM response time, and Co is the total value of the output capacitor(s).

Ideal simulation results of a 50A load increase for single phase and three phase converters is shown in figures 2 and 3 and shows the benefit of the multiphase approach. Input voltage is 12V, output voltage is 1.5V, and 0.5uH inductors, identical output capacitors and 250khz switching frequency are used for both converters. The PWM controller turn-on of the switch MOSFET is gated by a clock pulse from it's oscillator while turn-off can occur as required and is independent of the oscillator. The traces are from top down; output voltage (100mV/div), Electrolytic capacitor current (50A/div), Ceramic capacitor current (50A/div), and inductor current (50A/div). The time step is 4us per division.

**Figure 2 - Single Phase +50A Response**

![Figure 2 - Single Phase +50A Response](image)

**Figure 3 - Three Phase +50A Response**

![Figure 3 - Three Phase +50A Response](image)
It can be seen that the three-phase converter responds in about 4us while the single-phase converter requires about 6us. Multiphase helps in two ways; the inductor current has to increase to a smaller final value, and the turn-on delay is reduced due to the higher effective switching frequency.

Figures 4 and 5 compare how the same converters respond to a 50A load decrease. Response Time is much longer for both converters compared to the 50A load increase due to only 1.5V (the output voltage) instead of 10.5V (input -- output voltage) across the inductors. In this case, the 3-phase controller responds 3 times faster than the single phase due to no delay in response due to the oscillator. However, the delay caused by the oscillator did not have a significant effect on either converter as it is nearly compensated for by the increased inductor slew rate. It can also be seen in figure 2 through 5 that the multiphase converter has much lower output voltage ripple than the single-phase converter.

**Figure 4 - Single Phase minus 50A Response**

**Figure 5 - Three Phase minus 50A Response**
A technique known as Adaptive Voltage Positioning is often used to reduce the amount of bulk capacitance required to maintain the output voltage within its regulation limits during load transients. This approach positions the output voltage at a higher level under a light load and decreases it under a heavy load. The effect is to pre-charge the capacitors in anticipation of a load transient. Output voltage therefore varies with load current, increasing the effective impedance of the converter.

**Power MOSFETs**

The power MOSFETs used in multiphase buck converters for the switch and synchronous rectifier have different performance criteria. Due to the low duty cycle, the RDSon of the rectifier is its most important consideration as it conducts current during most of the switching cycle. Recently, MOSFETs with extremely low RDSon of only 2 to 3 milli-ohms have been introduced using trench technology. Most of this resistance is due to package interconnect and the PCB trace resistance may actually exceed that of the MOSFET! The penalty for this performance is threefold. First, trench tends to have considerable higher gate charge than planar technology. This leads to additional gate drive losses that are proportional to switching frequency. Second, the threshold voltage tends to be lower than planar with some devices being lower than 1V. While this would seem to be beneficial, it can pose considerable problems for the gate driver to turn them off, especially if there is any ringing following the switching transition. Finally the price of these newer devices is much higher although this can be expected to change in the future.

For the switch MOSFET, switching speed is the most important criteria to minimize switching losses. A low gate charge allows the gate driver to switch the FET more quickly. Although not usually specified, low gate resistance is also very important to achieve fast switching times. Planar MOSFETs with an RDSon of 10 to 20 milli-ohms are best for most applications today.

For both the switch and Synchronous MOSFET, a useful figure of merit when comparing components is the product of RDSon x Gate charge. Future advancements in multiphase technology will be dependent on manufactures significantly lowering this figure of merit.
MOSFET packaging is another important consideration. Small surface mount packages such as SO8 and DPAK are helpful when minimizing size is important, but their relatively high thermal impedance limits the ability to dissipate power. D2PAK is somewhat larger, but offers a lower thermal impedance that can be improved through the use of surface mount heatsinks. Although a through-hole technology, TO220 packages can be bolted to very large heatsinks resulting in extremely low thermal impedance if one can tolerate the required height and assembly cost. In some instances, thermal requirements lead to the use of two lower performance MOSFETs rather than with lower losses due to the inability to remove heat from the single package.

**Input Capacitors**

The Buck topology produces large peak currents on the input capacitors when the switch turns on. The multiphase approach significantly reduces the ripple current by dividing the load current by the number of phases and increasing the apparent duty cycle seen by the input capacitors. Figures 6, 7, and 8 show the input ripple current for 1, 2, and 3 phase converters with a 12V input, 2V output.

**Figure 6 - 1 phase Input Ripple Current**

![Figure 6 - 1 phase Input Ripple Current](image)

**Figure 7 - 2 phase Input Ripple Current**

![Figure 7 - 2 phase Input Ripple Current](image)

**Figure 8 - 3 phase Input Ripple Current**

![Figure 8 - 3 phase Input Ripple Current](image)
The input capacitors discharge when the switch is on, and charge when it is off. As the number of phases is increased, the discharge current is reduced while the charge current remains constant. The duty cycle for the single-phase converter is 1/6, which can be calculated from:

\[ D = \frac{V_{out}}{V_{in}} \] (4)

The apparent duty is duty cycle (4), multiplied by the number of phases. For the 2 phase, the apparent duty cycle is 1/3 and for the 3 phase it is 1/2. The input ripple current is minimized when the apparent duty cycle is 100%. For the example above, six phases would yield an apparent duty cycle of 100%.

If the output inductor ripple current is small, the RMS input current for apparent duty cycles of less than 1 can be calculated with the following equation:

\[ I_{RMS} = \sqrt{\left(I_{AVE} \times \left(\frac{1}{DA} - 1\right)\right)^2 \times DA + I_{AVE}^2 \times (1 - DA)^2} \] (5)

Input capacitors are usually selected based on their ripple current and voltage ratings. A capacitor's ripple current rating is based upon its parasitic ESR (equivalent series resistance) which causes power dissipation, and its physical size which determines their ability to dissipate heat. Low ESR electrolytic, organic, or tantalum capacitors are commonly used at the input of a multiphase converter. Multiple capacitors are usually paralleled to provide a high enough ripple current rating.

**Input Inductor**

An input inductor is often needed to keep the converter's input ripple current from injecting noise into the input bus, or to prevent the converter from exceeding the slew rate capability of the AC-DC power supply during load transients. This can cause the input capacitor voltage to droop during load transients, possibly requiring an increase in the value of input capacitance. The inductor should be sized so that its impedance is large enough to limit AC current flow at the converters effective switching frequency or during it's response time to a load transient.

**Output Inductor**
The output inductor and capacitors form a filter that provides a near DC voltage to the load. For the buck topology, the output capacitors see a continuous flow of current from the inductors, resulting in a much lower requirement to handle ripple current than the input capacitors. Multiphase converters further reduce the output ripple current through cancellation. As the inductor current in one-phase ramps up, currents in the other phase(s) ramp down and provide a canceling of currents during part of the switching cycle. Figure 9 shows ripple current waveforms for a three-phase 12V to 1.5V converter.

**Figure 9 - 12V to 1.5V 3 phase output filter ripple currents**

Output inductor ripple current is shown in the top section and output capacitor ripple in the bottom section. In a single-phase system the output inductor ripple is equal to the output capacitor ripple. Again, ripple would be minimized at the duty cycle when apparent duty cycle is one. Unlike the input filter capacitor which would never have peak-peak ripple less than the output inductor ripple, the output filter ripple ideally could be zero.

For steady state conditions when no more than one phase is on at any one time ripple can be calculated from Formula 5 where F is the frequency per phase,

\[
DI = (VIN - \#\text{Phases} \times VOUT) \times D / (L \times F) \tag{6}
\]

Selecting the value of the output inductor involves trading off ripple current, transient response, size, and cost. Lower inductor values improve transient response, but increase power loss in the input capacitors and MOSFETs and the ripple current seen by the output capacitors. For switching frequencies up to a few hundred kilohertz, inductors using low cost powered iron cores are a good choice. As frequencies increase, higher performance materials like ferrite are required to minimize core losses. Toroid cores are usually a good choice as they are inexpensive and have low EMI but are larger in size than rod or bobbin types and usually available as through hole components. Increasing the current per phase require a physically larger inductor to avoid saturating the core.
The majority of today's multiphase converters operating at frequencies below 500kHz have output inductor values in the range of 0.3 to 1.5uH.

**Output Capacitors**

The first task of the output capacitors is to control output voltage ripple. Usually the effective ESR of the capacitors (including the PCB) dominates their impedance. Output voltage ripple can therefore be calculated by multiplying the ripple current from equation (6) by the effective ESR. A good rule of thumb is that output voltage ripple should be no more than 1% of the output voltage.

The second task of the output capacitors is to maintain regulation during load transients and often determines their selection. Low ESR capacitors offering large values of capacitance include those based on organic electrolytic or Tantalum construction. Surface mount styles offer lower ESL than through hole versions. Although providing large hold-up time due to their ability to store charge, these capacitors can be physically large and suffer from relatively high ESL. Ceramic capacitors offer very low ESL, but are only available in values of 22uF or less and don't provide a lot of hold-up time. An effective solution can be to use a combination of low ESR capacitors for bulk charge storage and ceramics capacitors for fast response. The high ESL of electrolytic and tantalum capacitors makes them ineffective for switching frequencies greater than 500kHz.

**Power Loss and Thermal Management**

State-of-the-art multiphase converters deliver high currents to their low voltage outputs with excellent efficiency. However, significant amounts of power will still be wasted in the form of heat. A 2V/50A converter that achieves an efficiency of 90% will generate 10 watts of power dissipation. The resulting heat must be transferred to the ambient environment through a low impedance thermal path to avoid component stress and thermal runaway. The designer needs to determine the power dissipation and temperature rise in each component to ensure a reliable design. The power losses in multiphase buck converters mainly occur in the MOSFETs, Inductors, input capacitors, and gate drive circuit which can be a stand-alone IC or incorporated into the PWM control IC.

MOSFET Power Dissipation results from switching and conduction losses. In this case, one must consider the per phase inductor ripple current which can be calculated as follows:

\[
DI = (VIN - VOUT) \times D / (L \times F) \quad (7)
\]

The per phase inductor peak and valley currents are:

\[
I_{\text{peak}} = (I_{\text{out}} / \# \text{ of phases}) + DI/2 \quad (8)
\]

\[
I_{\text{valley}} = (I_{\text{out}} / \# \text{ of phases}) - DI/2 \quad (9)
\]

The per phase RMS current through the high side and low side MOSFETs are:

\[
I_{\text{RMS(H)}} = (I_{\text{peak}}^2 + (I_{\text{peak}} \times I_{\text{valley}}) + I_{\text{valley}}^2) \times D/31/2 \quad (10)
\]

\[
I_{\text{RMS(L)}} = (I_{\text{peak}}^2 + (I_{\text{peak}} \times I_{\text{valley}}) + I_{\text{valley}}^2) \times (1 - D)/31/2 \quad (11)
\]
The conduction losses in both the high and low side MOSFETs can be calculated from:

\[ \text{PCOND} = \text{IRMS}^2 \times \text{RDSon} \] (12)

If multiple MOSFETs are paralleled, the RMS current and RDSon are reduced accordingly.

Switching losses in the high side MOSFETs depend on the transition time between the on and off states. This is determined by the amount of drive current available to charge and discharge the MOSFET gate;

\[ \text{TT} = \frac{Q}{I} \] (13)

where \( Q \) is the total gate charge of the MOSFET(s) and is provided in the manufactures data sheet. High Side MOSFET switching losses can be estimated from;

\[ \text{PSW} = \frac{5}{16} \times \text{Iout} / \# \text{ phases} \times \text{Vin} \times \text{TT} \times F \] (14)

The low side MOSFET has very little switching losses since in its off state, the voltage across it is clamped by its body diode. It does suffer from losses due to body diode conduction, which can be calculated as;

\[ \text{PBD} = \text{Ivalley} \times \text{VF} \times \text{TOVLP} \] (15)

where \( \text{VF} \) is the body diode forward drop when conducting the inductor valley current and \( \text{TOVLP} \) is the non-overlap time. A schottky diode can be placed in parallel with the lower MOSFET(s) to reduce this loss.

Gate Drive losses for each MOSFET driver can be determined by

\[ \text{PDRV} = Q \times \text{VDRV} \times F \] (16)

where \( \text{VDRV} \) is the voltage applied to the MOSFET gate. This voltage must be greater than the input voltage plus the MOSFET threshold voltage in order to fully enhance the MOSFET.

Inductor power dissipation has two contributions, winding losses and core losses. Refer to the inductor manufactures data sheet to determine core losses. Winding losses can be calculated from;

\[ \text{PW} = (\text{Ipeak}^2 + (\text{Ipeak} \times \text{Ivalley}) + \text{Ivalley}^2) \times \text{wire resistance} \] (17)

Input Capacitor losses can be calculated by multiplying the square of their RMS current (equation 5) times their ESR.
Fault Protection

A robust design should provide an Undervoltage lockout circuit to ensure that adequate input and gate drive voltage is available. Failure to do so will cause the MOSFETs to operate in a linear mode rather than as low resistance switches and subject them to excessive stress and possible failure.

Softstart is required to prevent over-stress to the power components as they source excessive current to quickly charge the output capacitor. This can also cause a glitch in the input voltage and overshoot of output voltage.

Over-current protection is usually required to prevent damage to the converter if its output is inadvertently shorted. "Hiccup" protection where the converter shuts down for a period of time and then attempts to restart is usually preferred as this minimizes component stress and allows the system to restart once the over-current condition is removed.

MULTIPHASE BUCK DESIGN PROCEDURE

A suggested procedure for multiphase buck design;

1) Define the Converter Specifications 2) Select the number of Phases, Switching frequency, and Output Inductor value that best meet the specifications per the guidelines 3) Calculate the circuit parameters per the equations 4) Select Components 5) Layout

A multi-layer board with at least one ground plane is recommended. Output filter components should be placed on wide planes connected directly to the load to minimize drops during heavy loads and ringing during transients. Minimize the area of the inductor switching node by placing the inductor and MOSFETs for each phase close together. Traces with high currents and fast edges such as the inductor switching node and gate drive should be as short and wide as possible to minimize EMI. Place the input capacitors as close to the switching MOSFETs as possible, and the output capacitors as close to the load as possible.

6) Test the Design

MULTIPHASE BUCK DESIGN EXAMPLE

A 2-phase converter designed to power the AMD Athlon processor provides an example of a Multiphase Buck Converter. The specifications; schematic, Photograph of completed converter showing component placement, Bill of Materials and performance data of this converter follow:

Table 1. Power Supply Specifications
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Current</td>
<td>3 to 35A</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>5V +/- 5% for Bias</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1.6V</td>
</tr>
<tr>
<td>Output Voltage Stable Tolerance</td>
<td>+/- 50mV</td>
</tr>
<tr>
<td>Output Voltage Dynamic Tolerance</td>
<td>+/-100mV, +/-50mV</td>
</tr>
<tr>
<td>Output Load Current Slew Rate</td>
<td>300A/µs</td>
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<tr>
<td>Efficiency@ 35A</td>
<td>&gt; 80%</td>
</tr>
<tr>
<td>Efficiency@ 3A</td>
<td>&gt; 70%</td>
</tr>
<tr>
<td>Component Temperatures</td>
<td>&lt; 100°C</td>
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<tr>
<td>Construction</td>
<td>4 layer PCB, single side placement</td>
</tr>
</tbody>
</table>

**Figure 10 - Multiphase Schematic**

![Multiphase Schematic Diagram]

**Figure 11 - Photograph shows component placement**

![Component Placement Image]

**Table 2. Bill of Materials**

<table>
<thead>
<tr>
<th>Components</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>CSS302 PWM</td>
<td>Controller and Related Components</td>
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<tr>
<td>NE5532s (8)</td>
<td>DPAK</td>
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<td>Os-Cap Output Capacitors (12)</td>
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</tbody>
</table>

**Figure 12- Conversion Efficiency from 5V to 1.6V (Percent vs. Load Current)**

![Figure 12- Conversion Efficiency from 5V to 1.6V (Percent vs. Load Current)](image)

**Table 3. Component Temperatures**
<table>
<thead>
<tr>
<th>Location</th>
<th>38A Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient (no air flow)</td>
<td>27°C</td>
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<tr>
<td>U2</td>
<td>73°C</td>
</tr>
<tr>
<td>Q2</td>
<td>83°C</td>
</tr>
<tr>
<td>Q4</td>
<td>90°C</td>
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<tr>
<td>L2</td>
<td>87°C</td>
</tr>
<tr>
<td>C2</td>
<td>61°C</td>
</tr>
</tbody>
</table>

**Figure 13 - High Side Drivers and Output Ripple - No Load**

**Figure 14 - Output Inductor Current - 35A Load**

**Figure 15 - 3A to 35A Step Load (>20A/msec); Load Current, Input Current, Output Voltage**
REFERENCES


2 G. Schuellein, "Powering the Next-Gen Processor", Analog & Mixed Signal Applications Conference, October 1999