The relentless trend towards lower voltage, higher current and faster load slew rate poses a constant challenge for power supply designers. A decade ago, a typical power supply would have 5V and +/- 12V outputs. Obtaining reasonable efficiency and transient response within +/- 5 percent limit was rather straightforward. Relatively mature technologies of aluminum electrolytic capacitors and Schottky rectifiers were not leaving much room for error (or creativity). As the voltage required for a new generation of semiconductors had gone below 3.3V changes started to accelerate. Diodes were replaced by MOSFETs, several new types of high performance capacitors became available and new multiphase structures gained popularity with the advent of highly integrated controllers. The structure of the power systems shifted from a central to a distributed one. New categories of power supplies like Point of Load (POL) and VRM entered the mainstream market.

The most typical set of features of those new power supplies are as follows:

- high current, low voltage, single output

- close proximity to the load

- non isolated buck topology

- fast transient capability with narrow regulation band

- high level of integration with sophisticated PWM controllers

At the same time the availability of integrated controllers allowed engineers with just a basic power supply background to design high performance converters quickly and efficiently. On the surface, bringing to life a POL converter is simpler than an isolated telecomm brick or an AC/DC switcher. However, high and ever changing performance requirements, variety of new components and the relentless pressure on cost and cycle time make an optimization process a non trivial task. With the simplification of the structure, the bulk of the converter's losses is now located in the synchronous switching cell. The optimization of this part of the circuit is critical for achieving balance between the cost, size, efficiency and transient response capability. Several factors require a more detailed
look at the phenomenon of switching losses:

- the fast transient requirement pushes us towards possibly high switching frequencies, which in turn increases the relative importance of the switching losses

- switching processes of a synchronous cell are more complex than with a diode

- the selection of components is non-obvious (bigger does not have to be better) and has a critical impact on the performance

Let's take a look at several possible approaches to the task of estimating the switching losses in a synchronous buck converter.

**Method 1: Just do it.**

Years ago it was possible to achieve acceptable results without giving much thought to switching losses at all. With slowly changing technologies and fewer choices, the selection of typical MOSFETS with typical drivers and at a typical switching frequency could give us a solution not far from the one obtained after meticulous optimization. I have seen designers with a good track record working as follows: calculate the conduction losses, add 50 to 100% provision for switching losses and be done. This is undoubtedly the fastest and the cheapest of all methods. Currently obsolete, because nobody knows what typical components and typical frequency means.

**Method 2: Fall and rise time.**

Switching losses are created as a result of a simultaneous exposure of a MOSFET to high voltage and current during a transition between the open and closed states. Therefore, it is sufficient to know the duration and the type of a transition (for example resistive or inductive) and the calculation is straightforward:

**Figure 1: Idealized switching waveforms**

Idealized resistive switching $(PSW = 1/6 * FS * VDS * ID * TSW)$
Idealized inductive switching \( \text{Psw} = \frac{1}{2} \times \text{FS} \times \text{VDS} \times \text{ID} \times \text{TSW} \)

True, the real waveforms are a bit more complicated, but those errors can be within acceptable limits, providing that we are able to properly predict the rise and fall time of the drain to source voltage and the drain current. Those parameters can be found in the manufacturers’ datasheets. There are however numerous difficulties with obtaining accurate results in this way:

- components are described at one set of typical conditions, without an obvious method of conversion to another one - some parameters are characterized at unrealistic conditions because manufacturers do not have an equipment to perform measurements reliably in life-like setup (di/dt of the reverse recovery of a body diode with a low inductance layout can reach several thousand A/us, as opposed to 100 in datasheets)

- components are tested differently by various vendors, making direct comparison difficult

- timing is usually defined for the resistive switching which is convenient for manufacturers but has limited relevance for the inductive, diode clamping commutation taking place in the synchronous buck

- data is presented in a confusing way - for example fall time is defined as a time needed for drain to source voltage to rise from 10 to 90%

- last but not least some datasheets simply contain strange numbers

If we cannot obtain rise and fall times from manufacturers, we have to find them ourselves, hence the third approach:

**Method 3: Measure it**

The basic premise of this approach is that the switching phenomenon are just simply too complex to be accurately predicted. Therefore, we have to capture relevant waveforms in the working model and calculate the switching loss. This task used to involve a bit of computational effort, but with new oscilloscopes the whole math will be done for you. Just hook up the probes, sit back and relax...
Not so fast:

First: even very good current probes introduce a substantial delay in the waveforms. In the past 10 ns or so was not so important, but in the case of switching losses in a modern, fast dc/dc converter, capable of traversing from rail to rail in few nanoseconds it will lead to a completely false results. This delay can be estimated and proper correction introduced, but for fast switching circuits the error will remain huge.

Second: introducing a current probe into the circuit without disturbing a switching transition is sometimes very difficult. In the case of POL buck converters this act must increase the parasitic inductance of the switching cell significantly, thus distorting waveforms and making measurements inaccurate. Sometimes the converter will refuse to work completely.

Third: if anybody is not yet convinced of the limited usefulness of the measurement method, please consider this: in order to implement this method we have to have a working model of the power supply. If we get to this point we may just as well measure the overall efficiency and the temperatures of key components as a way of verifying of the design. After all, how important is the exact split of losses between switching and conduction, if the whole thing just works fine?

As we can see optimizing MOSFETS of a synchronous buck is not an easy task. Engineers do not have a luxury of time for detailed studies but trial and error method may turn out to be even more costly. A trade off between the accuracy of losses prediction and the amount of time and effort invested is necessary. Presented below approach is an attempt to balance accuracy with practical simplicity.

**Method 4: Calculation**

Upon closer examination the switching processes of the synchronous buck converter are surprisingly complex. We can easily distinguish 9 major components of these losses: conduction and gate charge losses for both switches, turn-on, turn-off and output capacitance losses for the forward MOSFET and body diode conduction plus body diode reverse recovery for the freewheeling MOSFET. Below, each of these components is analyzed in a greater detail and accompanied by the calculation for a "typical buck". For simplicity let's omit the second order impact of the ac inductor current.

Parameters used in the example:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>12 V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>1.6 V</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>15 A</td>
</tr>
<tr>
<td>$V_{GATE_FOR}$</td>
<td>10 V</td>
</tr>
<tr>
<td>$V_{GATE_FRE}$</td>
<td>6 V</td>
</tr>
<tr>
<td>$\eta$</td>
<td>85% (target)</td>
</tr>
<tr>
<td>Forward MOSFET</td>
<td>30 V, 7.0 mohm, 70 nC</td>
</tr>
<tr>
<td>Freewheeling MOSFET</td>
<td>30 V, 2.6 mohm, 16 nC</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>100 C</td>
</tr>
<tr>
<td>$R_{DR}$ - driver output resistance</td>
<td>4 Ohm</td>
</tr>
<tr>
<td>$R_{GATE}$ - MOSFET gate resistance</td>
<td>1.2 Ohm</td>
</tr>
<tr>
<td>$f_{SW}$ - switching frequency</td>
<td>500 kHz</td>
</tr>
</tbody>
</table>

Table 1
For the Freewheeling (synchronous, lower) MOSFET:

1. Conduction losses: 0.60 W

The losses caused by the flow of the current through the on resistance of the device during the freewheeling part of the switching cycle. Conduction process of the freewheeling MOSFET is a good place to start the calculations. It is the main component of the losses in this device and is relatively independent of the rest of the design.

\[ P_{c,dm} = I_{out}^2 \times (1-D) = R_{dson} = 0.60 \text{ W} \]

where \( D \) - duty cycle (\( D \approx \frac{V_{out}}{V_{in} \times \text{efficiency}} \)) \( R_{dson} \) - on resistance (consider the target temperature and gate voltage)

Typically the freewheeling MOSFET should have the \( R_{DSON} \) as low as possible within the space and budget constraints. For high frequency and silicon reach designs a balance must be achieved with the limitations imposed by an excessive gate charge.

2. Gate charge losses: 0.27 W

Energy lost due to periodic charging of the gate capacitance:

\[ P_{G} = FSW \times (Q_{GTOT} \times V_{GATE \ FREE} = 0.24 \text{ W} \text{ (at assumed } V_{GATE \ FREE} = 6 \text{ V}) \]

\( Q_{GTOT} \) - the total gate charge

It is sometimes mentioned in the literature that gate charge losses of the freewheeling MOSFET should be calculated without the Miller charge (approximated by the horizontal part of the gate charge chart). This is incorrect. The loss associated with the Miller charge is still present. It just occurs when the drain to source voltage swings, not when the driver changes its state. Figure 3: Gate charge chart with QGD - the Miller charge
The energy used to drive the gate of the device is lost unless a special recovery circuit is employed. This loss is divided between the gate driver and the MOSFET depending on the impedance ratio of those components. New generation MOSFETS typically have gate resistance in the 1 to 2 ohm range, much less than a mid size gate driver, so most heat ends up in the driver. *Frequently the ability of the driver to dissipate the heat will be a limiting factor for the selection of the freewheeling MOSFET.* The speed of switching, which is strongly affected by the size of the mosfet’s die is less critical because of the assistance of the body diode (except for the extreme case, when a very sloppy transition leads to an overlap with a drive signal of the upper MOSFET and shoot-through). Typically the lower Rdson, the bigger is the capacitance of the gate, the slower is the switching and the more loss is incurred for driving. New devices are also optimized for driving with lower gate voltage. Driving our freewheeling MOSFET to 12V would produce over 1 W of heat, exceeding the conduction component! If a lower gate voltage is not possible, a higher RDSON part may be necessary to keep the gate charge losses down.

3. **Body diode conduction losses: 0.45 W**

*Losses incurred during a brief period just before or just after the switching transition, during which the freewheeling MOSFET conducts the current with zero gate voltage.* This forces the current to flow in the internal body diode and has a significant impact on the efficiency because of a much higher voltage drop across the device during this period (and subsequently due to the energy loss for the reverse recovery):

\[
PBD = FSW \times VBD \times IOUT \times (TDEAD\ ON + TDEAD\ OFF) = 0.45\ W
\]

VBD - forward drop of the body diode (0.7 V in this case) TDEAD ON, TDEAD OFF - dead time in the gate driver (assume 100 ns total for on and off)

**Figure 4: Turn-on waveforms**
The dead time is mostly determined by the selection of the gate driver. It is not unusual to see 1 or even 2% difference in the overall efficiency due to the duration of the dead time. Most manufacturers prefer to insure ample dead time, because it minimizes the danger of cross-conduction (overlapping the on state of both devices) regardless of the MOSFET selection and layout. Cross-conduction may lead to a component failure, while too much dead time only to a slightly worsen performance. In order to avoid proliferation of parts with a variety of timing a conservative approach is preferred. This unfortunately leads to an under optimized design. In fact, operation with no dead time or even with minimal overlapping (cross-conduction) is the most efficient mode of operation.

The idea of switching at the boundary of cross-conduction (which is just a less pejorative word for shoot-through) requires a bit of explanation. The gain is threefold. First, the period during which the lossy body diode conducts is reduced. Second, as the conduction of the body diode is getting very short, the reverse recovery process is getting easier. It is because there is not enough time to fully saturate the junction with the excess carriers. Third, with further reduction of the dead time some of the current never gets to the body diode from the MOSFET's channel making the reverse recovery even more easy.

To achieve this mode of operation the gate drive timing must be very precisely adjusted to a particular design. What is even more difficult, it must be also adjusted with the line/load conditions and variations in the component properties. For this reasons such designs have been rare in the past. Currently new drivers, that actively sense the dynamics of the switching transition and adjust the dead time accordingly are becoming available. It should give good results providing that the operating conditions do not vary too rapidly from one cycle to another. Therefore we should approach this option carefully in the designs that have to change the duty cycle quickly due to a very fast transient response.

A widely known trick aimed to alleviate the body diode pains is the addition of a Schottk'y in parallel with the freewheeling MOSFET. This is meant to eliminate the current flow in the sloppy body diode and provide the benefit of almost instantaneous (lossless) reverse recovery of the Schottk'y. Unfortunately it works only at lower switching frequencies or with the Schottk'y integrated in one device with the MOSFET. The reason is simply the stray inductance between the MOSFET's channel and the Schottk'y causes a substantial amount of time to commutate the current. The body diode even though with a higher voltage drop is much closer. Let's assume that an average body diode has a voltage drop of 0.8V, Schottk'y only 0.4V and the inductance between them is only 4nH (an optimistic assumption). This means that the current will be shifting from the internal body diode to
the external Schottky at the rate of 1A per 10 ns. In our example we would have to wait for complete transition for 150 ns. This additional time would produce a lot of extra losses due to the body diode conduction which would cancel the benefits. Also the design of the controller may become complicated. A Schottky integrated in one package steals the space for the MOSFET, limiting its RDSON and therefore is applicable only for low current designs.

An external Schottky without a dead time extension is just a dead weight.

4. Body diode reverse recovery losses: 0.54 W (0.18 W in the freewheeling MOSFET)

Lossses incurred during reverse recovery of the body diode of the freewheeling device. The dynamics of this process are determined by the properties of the body diode, turn-on of the control MOSFET and the stray inductance in the triangle: forward MOSFET, freewheeling MOSFET and input capacitor (depicted as LSTRAY in Figure 2). A body diode is an inherently slow device and a substantial amount of reverse charge must be delivered during the recovery process (see the big current spike on the Figure 3). This charge is delivered under the voltage approximately equal to VIN and results in a large amount of power loss. It also extends the duration of the turn-on transition of the forward mosfet causing further degradation in efficiency. The calculation of these losses is difficult to conduct precisely because of poorly characterized properties of the body diode in the manufacturer's data. They also vary significantly with the temperature, forward current and the duration of the recovery process.

An error introduced by reverse recovery is usually the biggest factor behind inaccuracy of the overall prediction of the efficiency. It is however necessary to estimate the magnitude of this source of losses because of its significant contribution. If manufacturer specifies the reverse recovery charge QRR:

\[
PRR = FSW \times QRR \times VIN = 0.54 \text{ W}
\]

If only reverse recovery time at given di/dt is specified QRR can be then estimated as follows:

\[
IRR_{\text{PEAK}} = 0.6 \times \frac{\text{di/dt}}{} \times t_{RR} = 3.3 \text{ A - peak reverse recovery current} \quad IRR_{\text{AV}} = IRR_{\text{PEAK}} \times \frac{1}{2} = 1.65 \text{ A - average reverse recovery current} \quad QRR = IRR_{\text{AV}} \times t_{RR} = 91 \text{ nC - reverse recovery charge}
\]

It is difficult to determine how the heat generated during the reverse recovery process splits between both devices. Lets say 1/3 of the power is dissipated in the body diode (freewheeling MOSFET), 1/2 in the forward MOSFET and 1/6 in the rest of the circuit, but it will vary from case to case.

See more information about optimizing the reverse recovery losses in section describing turn-on of the forward MOSFET.

5. Turn-on losses 0 W
Turn-on losses are here understood as a simultaneous exposure of the component to a significant voltage and current experienced during turn-on of the device. There are no turn-on losses of the freewheeling MOSFET because it turns-on at zero voltage. The commutation process is forced by the energy stored in the choke.

6. Turn-off losses 0 W

Turn-off losses are here understood as a simultaneous exposure of the component to a significant voltage and current experienced during turn-off of the device. Similarly turn-off losses are zero, because of the assistance of the body diode.

7. Output capacitance losses 0 W

Output capacitance losses are the losses resulting from dissipating the energy stored in the output capacitance of the MOSFET during turn-on. Output capacitance losses are 0 because this energy is recycled by the choke. In other words the freewheeling MOSFET turns-on at zero voltage.

Forward (control, upper) MOSFET:

8. Turn-off losses: 0.65 W

Occur briefly during the switching transition when the device passes through the active region. These losses may be divided into three major stages:

Stage 0: the gate voltage starts to go down and as a result the resistance of the channel is also gradually increasing. As the gate voltage changes from its steady state value of about 10 V to 3 V no significant increase of the drain to source voltage occurs. Gradually increasing the resistance of the channel however results in some additional losses in comparison to the fully enhanced state. Computation of these losses is possible if we know the relationship between the gate voltage and \( R_{Dson} \) and know the rate of change of the gate voltage from the properties of our driver circuit and the nonlinear gate capacitance characteristic. The above information is usually poorly represented in manufacturer's datasheets but luckily this exercise can be totally skipped because these losses are
Stage I: as the gate voltage continues to descend, the increasing resistance of the channel finally causes the drain to source voltage to move. As this is happening the Miller effect keeps the gate voltage at a constant level (almost). This state will last until the driver manages to remove the drain to gate charge QGD (representing the Miller capacitance): IDR = VPT/( RDR + RGATE) = 0.5 A (gate discharge current at plateau level)

TOFF 1 = QGD / IDR = 12 ns VPT = Vplateau: the gate voltage at which the resistance of the channel increased to the point where the drain to source voltage starts to rise rapidly (a characteristic plateau at the gate charge to gate voltage chart - 2.5V in this case)

Stage I end when QGD is removed from the gate. By definition, at the same time the drain to source will reach Vin and the drain current will start to decrease. Stage I losses are important and can be calculated with reasonable accuracy. Assumption about linear rise of the voltage in Stage I causes only second order error because CISS changes only slightly with the drain to source voltage. The losses can be computed as follows:

POFF 1 = FSW * TOFF 1 * 1/2 * VIN * IOUT = 0.54 W

Stage II: After the drain to source voltage exceeds VIN, the freewheeling device is becoming positively biased and starts conducting the current. The commutation is not instantaneous. Since the resistance of the channel is far from full on state, some current continues to flow in the forward MOSFET and only gradually is shifting to the freewheeling device. The duration of this phase will be proportional to the rate of increase of the resistance of the MOSFET with the gate voltages below plateau. It will depend on the properties of the MOSFET and the driver at low gate voltages. Some manufacturers are recently starting to provide more information allowing us to characterize this process.

If we are lucky we will have the gate charge representing this stage, most commonly referred to as QGS2. So:

IDR = 1/2 * (VPT + VTH)/( RDR + RGATE) = 0.38 A

(an average driver current - good approximation if VTH is not less then 1/2 of VPT)

TOFF 2 = QGS2/IDR = 2.5 ns (assumes constant CISS - small error)

POFF 2 = FSW * TOFF 2 * 1/2 * VIN * IOUT = 0.11 W

It is important to remember that QGS2 changes strongly with the drain current. Typically we would have this parameter specified for only one, typical current. For different conditions we can assume, with reasonable accuracy, that the QGS2 changes proportionally with the magnitude of the drain
If QGS2 is not available we can estimate it with reasonable accuracy assuming that the phase II lasts from the moment when the gate voltage goes below the plateau level until it reaches the threshold level and the drain current decreases linearly (threshold voltage is always present in manufacturers datasheets).

QGS2 = (VPT - VTH)/VPT) * QGS

Those striving the best possible accuracy may find worthwhile to calculate the losses in phase II from the chart showing the saturation current depending on the drain to source and gate to source voltages:

**Figure 6: IDRAIN versus VDS chart**

![IDRAIN versus VDS chart](image)

From this chart we can extract the information about the relationship between the drain current and the gate voltage for given drain to source voltage (in our case 12V). Knowing the gate discharge current we know the rate of change of the gate voltage and the rate of change of the current. Losses experienced in phase II are usually several times smaller than in phase I, but they may vary significantly from one device to another.

*The actual losses during the turn-off are actually larger than the above number due to the energy stored in the stray inductance. It is however practical to disregard this factor because it is the energy that was subtracted from the losses during turn-on. In other words, we are underestimating the turn-off losses by the similar amount we have overestimated the turn-on losses. The parasitic inductance makes the turn-off harder but the turn-on easier.*

**9. Turn-on losses: 0.54 W**

*Turn-on losses are the result of a simultaneous exposure of the component to a large voltage and current during turn-on. These losses are significant for the forward MOSFET as can be seen from Figure 3. Similarly like with the turn-off the speed with which the transistor travels through the active region will determine the amount of losses. Here however we do not have a full freedom to*
speed up this process as much as possible.

*It is because the resistive voltage drop across the forward MOSFET and the layout inductance LSTRAY are the main factors limiting the speed of the reverse recovery process of the lower MOSFET's body diode. The optimal turn-on of the upper MOSFET is relatively slow and in most cases measures should be taken to avoid too speedy transition. This is particularly important if we realize that due to a low plateau level in modern devices the turn-on current of the gate driver tends to be higher than the turn-off current (and we want turn-off current to be as high as possible). Shifting to a more powerful gate driver will reduce the turn-off losses, but may actually make reverse recovery losses worse! With an unfavorable combination of factors this may lead to ringing at the gate of both MOSFETs, then multiple switching transitions, shoot-through and the destruction of the semiconductors!*

Let's note that the body diode needs a fixed (roughly) amount of charge to recover its voltage blocking capabilities. Speeding up the upper MOSFET's turn-on will shorten the reverse recovery process but at the expense of higher peak current.

*Interestingly, against the common wisdom, the parasitic inductance of the layout LSTRAY plays a positive role during the turn-on of the upper MOSFET. It slows down the rate of the rise of the reverse recovery current, allowing the body diode to recover with lower peak current. This lower peak current results in a lower dv/dt of the drain to source voltage when the body diode finally snaps in. Conversely, fast turn-on of the forward MOSFET, combined with a very low inductance layout results in a very abrupt reverse recover process with multiple nasty side effects:*

- high current stress on the forward MOSFET
- strong source of an inductively coupled noise
- higher voltage spike on the freewheeling MOSFET when the diode recovers
- high frequency ringing producing a capacitively coupled noise
- voltage stress of the gate driver - spike may sometimes damage the driver before it hurts the MOSFET
- so called dv/dt induced turn-on of the freewheeling MOSFET via Miller capacitance (see VGS jump on Figure 3)
- disturbs the turn-on process of the upper MOSFET via the same Miller capacitance (see VGS dip on Figure 3)

The last two issues are particularly dangerous. The mechanism is as follows. Rapid turn-on of the control MOSFET creates a large reverse recovery current. When the diode regains blocking
capability the energy stored in the stray inductance of the circuit keeps the current flowing. This current, plus the resonance of the stray inductance with the output capacitance of the MOSFET creates a very rapid rise of the drain to source voltage. This voltage in turn couples to the gate of the lower MOSFET via a Miller capacitance and forces the gate voltage to rise. What we have is in fact a capacitive divider consisting of a gate to drain and gate to source capacitance. Of course the gate driver is trying to keep the gate off, but with the threshold levels of modern components below 2V only a driver with negative voltage capability is a certain way of keeping the device off.

The nasty consequences are easy to imagine. We will observe a brief shoot-through following the reverse recovery. Typically the shoot-through current spike will follow a reverse recovery closely creating one, big, extended current spike. If the layout introduces substantial amounts of inductance in the gate circuit we will observe ringing. This ringing may exceed the threshold level and cause the freewheeling MOSFET to traveling through an active region multiple times. Such operation will lead to large losses and a possible destruction of the components.

A similar mechanism can be observed for the upper MOSFET. This time however the rapid rise of the drain to source voltage forces the transistor to turn-off in the middle of the turn-on process increasing the stress on the component.

The above phenomenon are not possible to eliminate entirely but have to be kept at a reasonable level. First we have to slow down the turn-on of the forward MOSFET. Luckily it is easy to do. We just have to put a resistor in series with the bootstrap capacitor. This will reduce the turn-on current without affecting the turn-off. We can also adjust the voltage of the upper MOSFET driver by selecting a small boot-strap capacitance. Second, let’s not go overboard with reducing the layout inductance. It will take some burden of the forward MOSFET during turn-on. Third, use snubbers to slow down dv/dt (reducing coupling via Miller capacitance) and dampening the ringing.

While checking the reverse recovery we have to remember that, particularly with a low parasitic inductance layout, the voltage spike may be extremely narrow. It may last only few nanoseconds but can easily exceed 30 V with input voltage of 12 V. The waveform will look quite naturally on a 100 MHz oscilloscope but observed voltage stress will be much lower than the actual one. To really see what is happening we need at least solid 300 MHz, 1Gs/s and adequate probes.

The question is still open if low energy spikes approaching or exceeding the maximum rating of the MOSFET are a substantial danger to the reliability. It seems that there is a consensus that for a short time practically all modern devices are capable of withstanding limited energy avalanching. There are however no conclusive studies about the long term impact. (low cost VRMs frequently use 20 V MOSFETS, then such stress is difficult to avoid).

The hard part is how to calculate the turn-on losses during the transition accompanied by the reverse recovery of the body diode. Please note that that the duration of this process is now determined more by the reverse recovery process than by the driver capabilities. In particular it is not correct to use the QGS2 to calculate the duration of this process and the resulting losses in the same manner as for turn-off (as suggested sometimes in the literature). Please note that QGS2 depends strongly on the magnitude of the commutated current. The current that should be used for calculations here is the sum of the load current and the reverse recovery current, which is practically unknown. Also the layout parasitic inductance has a significant influence on the dynamics.
of the process. However, it turns out that with practical, medium speed turn-on transition a good approximation of turn-on losses is just to make them equal to the reverse recovery losses! (explanation of this is beyond the scope of this article).

\[
PON = PRR = 0.54 \text{ W}
\]

Below are the basic rules of avoiding reverse recovery troubles.

- shop for a good body diode with a low reverse recovery charge and soft characteristic (not easy but manufacturers are starting to pay some attention to this subject)

- keep the dead time short, the reverse recovery will be easier if the body diode conducts very briefly

- slow down the turn-on of the upper MOSFET to give enough time for the reverse recovery without a huge current spike, 12 to 15 ns is a good starting point

- select the freewheeling MOSFET with a high ratio of QGS to QGD (to reduce the di/dt turn-on)

- make sure that the lower driver is effective in keeping the gate voltage low, in extreme cases consider using a negative turn-off voltage

- keep the parasitic inductance at a moderate level

- consider using a MOSFET with an integrated Schottk'y diode, it will have a negligible reverse recovery current thus eliminating the problem - option available only for low current design

- use solid snubbers - suppressed ringing will make gate signals much cleaner and prevent unwanted transitions

For special applications operating at frequencies above 500kHz integrated devices containing gate driver and two MOSFETS in one package are becoming an interesting alternative. For various reasons such devices have difficulties in realizing their potential coming from reduced parasitics and perfectly matched components. As of today discrete solutions can still keep up with their performance at lower cost.

\textbf{10. Freewheeling body diode reverse recovery losses: 0.27 W} (1/2 of the losses analyzed for a freewheeling MOSFET)

\textbf{11. Conduction losses: 0.26 W}

\[
PCOND = IOUT2 \times (1-D) \times RdSON = 0.26 \text{ W}
\]
12. **Gate charge losses: 0.15 W**

\[ PGD = FSW \times Q_{TOT} \times \frac{V_{GMAX}}{0.15W} \text{ (assumed } V_{GMAX} = 10V) \]

Most of the gate charge losses will show up in the gate driver.

13. **Output capacitance losses: 0.026 W**

*The energy stored in the output capacitance of the MOSFETS and dissipated during turn-on.* Since the output capacitance is a strong function of the drain to source voltage the proper way to calculate this power is as follows: \[ PCAP = FSW \times COSS (V) \times \frac{V_{dV}}{V} \text{ (forward)} \]

\[ COSS (V) \] - output capacitance of the MOSFET

This task is a bit involved since \( COSS(V) \) is a strongly non linear function, which must be restored from the graph in manufacturers data sheet or extracted from the simulation model and then integrated in a piecewise fashion. For quick and dirty estimations it is better to use the approximation: \[ COSS = \frac{4}{3} \times COSS (V_{in}) \]

Hence the capacitive turn-on losses:

\[ PCAP = FSW \times \frac{1}{2} \times \frac{4}{3} \times COSS (V_{in}) \times V_{in}^2 = 0.026 W \]

This is a negligible value, as expected for a low voltage device. These losses can be totally skipped unless higher a voltage or extreme frequency is used.

**Summary:**

Total losses in the forward MOSFET:

\[ P_{forw} = 1.89 W \]

Total losses in the freewheeling MOSFET:

\[ P_{forw} = 1.50 W \]

Assuming that the losses in the remaining part of the circuit are 1 W (ambitious but possible), the overall efficiency is 84.5%. Reasonably balanced losses indicate that the above solution is probably not very far from optimal.
How to make it better? Presented above calculations suggest where one should look for potential improvements:

1. Properly select both MOSFETS depending on the operating condition of the circuit. The forward MOSFET should be fast (for fast turn-off), while the freewheeling MOSFET with low resistance. Oversizing in both places may result in lower efficiency, but particular attention should be given to the forward MOSFET. Too large die (very low RDSON) will result in reduced efficiency.

2. Reduce the dead time of the gate driver to minimum. It will decrease body diode conduction losses. If the dead time is near zero also the losses due to the reverse recovery of the body diode can be greatly reduced. In fact a small amount of shoot-through is the most efficient arrangement. Such precise adjustment however; requires gate driver timing varying with the load, input voltage, temperature, layout, etc. - an adaptive or predictive gate driver must be used. Luckily, integrated drivers of this kind are becoming available.

3. Use gate drivers with sufficient "oomph". Particularly with the modern devices a low threshold level makes the turn-off of the forward MOSFET difficult. Using negative voltage for turn-off seems to be a viable option for the high frequency designs.

4. Optimize the gate driver voltage if possible to reduce gate charge losses.

5. Keep MOSFETs possibly well cooled. High temperature increases RDSON and makes the reverse recovery of the body diode worse.

6. Consider a parallel Schottk'y only if integrated in one package with a freewheeling MOSFET.

7. Use low switching frequency unless impossible due to the volume and/or transient response.

8. Lower the input voltage if possible to reduce the switching losses.

9. Use low resistance 20V MOSFETS if possible (it is difficult to keep the turn-off spike from approaching the maximum rating with 12V input).

10. Harness the destructive forces of the layout stray inductance and make them work for you, not against you.

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