Low-cost FPGA-based SPI-4.2 solution from Lattice

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The chaps and chappesses at Lattice Semiconductor have just announced the immediate availability of their full rate SPI-4.2 solution based on a low-cost, low-power FPGA fabric.

Consisting of a LatticeECP3 FPGA and a Lattice-developed soft Intellectual Property (IP) core, the solution is fully compliant with the Optical Internetworking Forum’s (OIF) System Packet Interface Level 4 (SPI-4) Phase 2 Revision 1 Standard, a popular parallel interface found in telecom/datacom applications at 10Gbps rates and below.

The ability to operate at the full 10Gbps line rate is made possible by Lattice’s sysI/O interface structure, which contains pre-engineered elements designed to support the implementation of very fast, source synchronous interfaces such as high speed DDR2 and DDR3 memory interfaces and SPI-4.2. By delivering high-end FPGA features and performance in its award winning LatticeECP3 FPGA fabric, Lattice is able to provide telecom customers with a low power, low cost SPI4.2 solution for line card applications.

Lattice’s SPI-4.2 solution is supported by Lattice’s IPexpress FPGA design tool module. Included as a standard feature in the Lattice Diamond design tool suite, the IPexpress module significantly reduces design time by allowing IP parameterization and timing analysis on the designer’s desktop. This allows users to customize Lattice’s extensive library of IP functions for their unique applications, integrate them with their proprietary FPGA logic designs and evaluate the overall device operation via simulation and timing analysis prior to making any IP purchase commitments.

An FPGA-based SPI-4.2 solution provides system designers with a flexible way to support intelligent bridging functions interfacing with today’s high-performance communications ASSPs, including network processors, traffic managers, MACs, or framers. The problem is that, until now, designers typically needed to use more expensive FPGA devices to implement full rate SPI-4.2 bridges.
supporting complex packet flow and traffic management policies. The folks at Lattice say that the combination of the LatticeECP3 FPGA and their SPI-4.2 IP core changes the game by providing designers with a low-cost, low-power SPI4.2 solution.

The new SPI-4.2 soft IP core requires about 4000 FPGA look-up tables (LUTs) in 128-bit mode for a full 256-channel static mode core. It therefore can be implemented along with other user logic in all LatticeECP3 family members, from the LatticeECP3-17 device through the largest member of the family, the LatticeECP3-150 device. The SPI-4.2 core operates at interface speeds of up to 11.2 Gbps while fulfilling all requirements of the SPI-4.2 interface protocol, including support for up to 256 logic channels, calendars, transmit and receive status, programmable burst size, and DIP4 error checking.

**Pricing and availability**
With a list price of $3,000, the SPI-4.2 IP core is available now and can be ordered through Lattice sales: [www.latticesemi.com/sales](http://www.latticesemi.com/sales). ([Click Here](http://www.latticesemi.com/sales) for more information on the SPI-4.2 soft IP core).