At-Speed Test Methods for LSSD and Mux Flip-Flop Designs – Best Practices

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Abstract
At-speed scan testing has become necessary to detect the growing population of timing defects in today’s nanometer-scale process. There are several at-speed delay test methods available in the industry to generate the delay patterns. Manufacturers are continuing to look for ways to improve the effectiveness of at-speed delay test. The key is to create high quality, cost effective tests for these complex nanometer designs.

This paper describes an efficient at-speed test implementation technique known as improved launch delay test with level sensitive scan design (LSSD) and mux scan flip-flop design which in turn achieve high quality cost effective delay test patterns. The importance of small delay defect testing and sources of chip overkill are also brought together in this paper as they are inevitable factors with at-speed test techniques. At the end of the paper the best suitable flow and recommendations for the optimized patterns with good coverage during at-speed testing are explained.

Keywords
DFT, ATPG, Capture cycle, At-speed test, Launch-off-Capture, Launch-off-Shift, Design with Test.

1. Introduction
At-speed test has become a common method to ensure fault-free high performance chips to the customers. For DSM designs, the stuck-at fault test alone cannot ensure high quality level of chips. In the past, functional patterns were used for at-speed test. However, functional testing is not a viable solution because of the difficulty and time to generate these tests for complex designs with very high gate density.

The two common methods used for generating delay patterns are called Launch off Shift and Launch off Capture.

For at-speed test, the LOS (Launch-off-Shift) scheme can easily justify the launch values as the launch data is derived from the output of the previous scan element in the scan chain rather than the output of logical cones in the functional path. This LOS method makes the ATPG easier and it can offer fewer at-speed patterns. The main drawback with this approach is the tight constraints to build the scan enable clock tree and the tight primary input timing requirements during capture phase. The synchronization of the at-speed scan enable switching with the at-speed internal clocks (derived from PLL) is a difficult design challenge in LOS. LOS pattern can result in better optimization if the at-speed timing of scan enable can be met.

In launch-off-capture (LOC) scheme, the entire scan data shifting can be done at slow speeds in test mode, and then two at-speed clocks are pulsed for launch and capture in functional mode. In this approach, there is no timing requirement for the scan enable as functional justification is used to generate the delay patterns (fast sequential patterns). This LOC method demands more patterns with medium fault coverage.

This paper describes the improved launch delay testing with extra shifts/skewed load for mux flip-flop and level sensitive scan design (LSSD) circuits. It also provides information about the inevitable factors during delay test such as the timing aware ATPG which is used to target small delay defects and chip overkill issues which leads to unnecessary loss of yield. Finally it is concluded by recommending a suitable flow for optimized patterns with good coverage during delay faults pattern generation.

2. At-speed Test - Best Practices
This session covers the efficient practices for LSSD and mux scan Flip-flop at-speed delay tests.

2.1 LSSD Design At-Speed Test
The fundamental SRL (Serial Register Latch) consists of two latches (master and slave) operated by a pair of non-overlapping clocks called A and B clock to shift data. Level Sensitive Scan Design (LSSD) provides scan designs with race free clocking. All latches in LSSD are implemented as part of SRL as shown in figure 1. The basic storage element (SRL) consists of L1 and L2 latches (Latch pairs). The L1 has a system data port controlled by a system C1 clock and a shift A clock. The L2 has a single data port controlled by System C2/B shift clocks. At-speed test with LSSD designs is to apply launch and capture clocks at system speed. The time interval between the rising edge of C2 clock (launch event) and trailing edge of C1 system
clock (capture event) must be same as system speed. The LOC and LOS approaches can be used in LSSD but there are drawbacks as discussed earlier in introduction.

**Figure 1: LSSD (Double Latch Device)**

In LSSD designs, separate clocks are used for the launch and capture so that the tests are not limited by the scan enable timing / tester frequency. The figure 2 shows at-speed clock sequence where master will be loaded to a value which opposes the slave latch value data. In this scheme (similar to LOC), functional justification is used to generate master load vectors as the SE signal asserted low. This approach demands more patterns (fast sequential patterns) and provides only medium fault coverage.

**Figure 2: LSSD At-Speed with functional justification**

It is always easy for the ATPG tools to derive the launch patterns from the scan shift chains. Figure 3 shows such an effort for an efficient LSSD at-speed test. In this clock sequence, patterns are shifted as usual, but at the end with an extra A shift clock so that the L1 or master latch can be loaded to a value that is opposite to that of L2 or slave latch. The main advantage is that only fewer patterns are required since many tests can be setup by setting opposing values in the master and slave latches. Also there is no faster scan enable (SE) timing requirement.

**Figure 3: LSSD At-speed test with skewed load**

Even though the above skewed load approach provide fewer patterns with high coverage, it is important to avoid the source of over kill (good chips may fail with scan test) such as multi cycle paths, long false paths, excessive switching activities, etc. These cases are explained in detail later.

**2.2. Mux Flip-flop At-Speed Test**

In edge triggered mux scan designs, LOS method can be used to justify the launch values from the output of the previous scan element in the scan chain. But the main disadvantage is the requirement of high speed scan enable. This drawback can be overcome by using pipelined local scan enable.

The figures 4, 5 show the waveform and the scan enable pipelining circuit requirement with improved launch delay scheme. As shown in the figure, the scan enable pipe-lining circuitry in the design holds the local scan enable active high during the launch cycle and then goes inactive low during the capture cycle.

**Figure 4: Mux FF At-Speed with Extra Shift**
In this improved scheme, the scan chains are loaded completely and the launch clock causes an extra shift but this really looks like a regular launch on capture clock from the chip top level. The scan chains get a single pipe-line-delayed scan enable signal which is the same clock driving the flip-flops in the scan chains.

So in mux scan flip flop designs, the location and the number of pipeline registers are to be carefully considered to meet system speed timing, to avoid congestion and to limit the test area overhead. The SE signal must also to be properly constrained during synthesis, physical implementation and timing analysis steps.

2.3. Small Delay Defect Testing is a must
As design sizes and frequency of operation increases, more and more circuit nodes will be susceptible to a small delay defect. Detection of a transition fault is independent of which path is used to sensitize and propagate the fault. But a longer path will have a smaller slack and will be more sensitive to the additional delay caused by an at-speed defect. Specifically, a small delay defect could be missed if a shorter path is used for detecting transition fault.

SDD test is an extension to the basic transition fault model capturing transition faults through the longest timing path. In this technique, the at-speed test pattern set is more likely to detect small defects that could escape a normal transition test set. If it can be guaranteed that SDD will always detect the fault along the longest path, then SDD will also serve the purpose of path delay, thereby eliminating the need for path delay test. The efficacy of the small delay defect test is always higher with higher pattern count. Higher pattern count can be limited by the improved launch delay testing methods as discussed earlier. Also fault grading techniques are to be considered for reducing the overall test volume.

3. Over Testing can Overkill
Any scan based test can generate vectors to test the faults that are not sensitized in a functional mode which is always potential issue. Multi-cycle and false paths are not intended to propagate signals within one clock cycle during normal functional operation. They also can be erroneously sensitized during scan pattern generation. This in turn could cause some good dies to fail the test by exercising functionally unsensitizable path, thus leading to unnecessary loss of yield (overkill the device).

The figure 7 shows a sample design with functionally unsensitizable path (refer only the functional path). In this circuit, any transition at the starting point never reaches the end of the path and so these types of paths are never functionally exercised. Same cases can occur when no transition occurs at the start point of the
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path or when captured values at the end are never propagated to any primary output. These types of paths are untestable in the original circuit but after the DFT insertion all these type of circuit will become testable.

Figure 7: Functional unsensitizable path

As described before improved launch delay with extra shift/skewed load scheme also can justify the launch values as the launch data derives from the output of the previous scan elements. So in this method, it’s important to avoid over testing by identifying the false at speed transitions.

Another important factor that can overkill the device is the excessive power during test. Since the capture cycle is operated at-speed for high speed defect detection, the frequency of occurrence of high di/dt also increases. Combined with high speed, the effects of excessive VDD-drop and ground-bounce could possibly change the logic states of some circuit nodes erroneously. This in turn could cause some good dies to fail the test, thus leading to unnecessary loss of yield.

4. At-Speed Test - Best Flow

Test insertion can make functionally non-testable path testable so a very well optimized non scan inserted net list is essential to get a high quality results with Extra Shift Launch Delay Test method. In other means, both improved Launch delay test with extra shift and functional justification Launch-Off-Capture (LOC) method should have almost same type/number of untestable faults and almost same coverage. But extra shift launch delay testing scheme should provide a reduced pattern set as the difference in the launch procedure.

For an efficient at speed implementation, the flow should start with a well optimized non-scan inserted net list. Then a proper analysis of untestable faults list has to done as shown in the flow diagram (Figure 8).

Figure 8: At speed test – Best Flow

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**Figure 7:** Functional unsensitizable path

**Figure 8:** At speed test – Best Flow
Finally the at-speed patterns with extra shift LOS scheme have to be generated with power and timing aware constraints.

5. Conclusion

This paper explains the improved delay at speed testing technique (extra shift/skewed load) for LSSD and mux scan flip flop designs. It also covers few concerns with this approach and the best suitable delay test flow for nanometer devices. An optimized delay pattern with a high coverage is the key to reduce the test cost without compromising the quality. Improved Launch delay test maximizes the amount of data that can be launched in the extra shift which will in turn result in a smaller pattern set. As small delay defect (SDD) testing is essential in nanometer devices, it is recommended to use this hybrid launch delay technique so as to bring down the overall at-speed pattern count.

Local scan enable timing requirement is critical in mux scan FF designs with enhanced launch delay at-speed test. So the placement of scan enable pipeline registers and the number of SE pipelining registers have to be considered carefully. Chip overkill factors are also very crucial in any at speed test method, so a very well optimized non scan inserted net list, ATPG untestable fault category evaluations, multi cycle path, long false paths considerations and test power reductions have to be taken into consideration while implementing the at-speed test.

6. References


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