Magillem Verification Scenarii environment configures validation of IP, sub-systems, and testbench generation

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Magillem Verification Scenarii, is the latest software proudly launched by Magillem, the leader of IP XACT based solutions for improved flow methodology:

Complex SoCs require three layers of partitioning: functional sub systems with configurable parameters for architects, logical blocks (hierarchical assembly for implementation) used by designers and integrators, and functional validation subsets necessary for verification teams.

MVS is dedicated to those validation teams. Once IP and VIP blocks have been packaged in IP XACT, the SoC has been assembled with Magillem Platform Assembly (MPA), the registers have been captured with Magillem Register View (MRV), the sequences have been written by firmware engineers thanks to Magillem Sequence Editor (MSE), test teams need an environment to configure IP and sub systems they want to validate, and to automate the generation of the test bench: system clocks, hardware sequences, monitor and probes insertion, file set for compilation and simulation...this environment is provided by MVS and its generators.

MVS offers a GUI mode and a CLI mode. The graphical mode makes it easy for the engineer to select and configure their test bench

MVS offers a Sequence Editor based on MSE to write functional sequences matching specification configuration and to run the tests on registers.

If MRV has been used to capture registers, it is also possible to generate register connectivity tests, in order to verify registers access as defined in the specification.

MVS is leveraging the IP XACT XML metadata, as it allows to access all facets of each IP, each facet can show a different language at multiple abstraction levels, VHDL, Verilog, System C, e language, System Verilog, as defined for each step of the flow. Without IP XACT, managing the IP database is much more complicated, and requires regenerating the test bench before compiling for each simulation tool.

Thanks to the use of IP XACT, MVS provides a single API to handle all the resources of an IP or a platform at once. Time savings are invaluable! Various validation strategies can be implemented without duplicating efforts (OVM, UVM...). For example, a sub system can be tested for one set of parameters with Cadence Incisive Enterprise Simulator ™ while the top level will be running on Mentor Questa™.
"MVS is a no-learning-curve add-on for all our customers already familiar with the Magillem software suite, now the one-stop-shopping front end environment for IP reuse based design strategies. Verification engineers will enhance and change their flow very easily to adapt it to new challenges posed by very large SOCs" says Cyril Spasevski, CTO and co founder of MAGILLEM."MVS has been extensively tested by two of our largest customers among the top 6 in the semiconductor industry, both designing an ARM based complex SOC, and they are raving about their improved performance, quality of verification and time efficiency."

**About Magillem**
Magillem, a board member of ACCELLERA™, has developed an easy to use, IP-XACT based state-of-the-art platform solution to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SOC. Company is Headquartered in Paris, France, with offices in New York, USA and Tokyo, Japan. Customers include the first tier SoC manufacturers worldwide. Magillem is a public company traded on the Euronext Free Market.

**About IP-XACT / IEEE 1685™**

IP-XACT was created by the SPIRIT Consortium, now part of Accellera, as a standard to enable automated configuration and integration through tools. 150 industrial companies and organizations are members. The goals of the standard are: to ensure delivery of compatible component descriptions from multiple component vendors, to enable exchanging complex component libraries between electronic design automation (EDA) tools for SoC design (design environments), to describe configurable components using metadata, and to enable the provision of EDA vendor neutral scripts for component creation and configuration.

For further information please visit [www.magillem.com](http://www.magillem.com)