Xilinx connectivity IP cores for next-gen LTE/LTE-A wireless infrastructure

Clive (Max) Maxfield - November 16, 2011

The folks at Xilinx have just announced the availability of three key connectivity IP cores that they say are vital for building programmable, flexible and cost effective 3G+/4G wireless base stations.

Xilinx’s Serial RapidIO Gen 2 v1.2 Endpoint LogiCORE IP, JESD204 v1.1 LogiCORE IP, and CPRI v4.1 LogiCORE IP all support connectivity standards and will help developers address design challenges in building new wireless equipment with higher system capacities.

The growth in the number of wireless broadband data users and consumption demands is making today’s wireless infrastructure network inadequate. With mobile broadband users expected to grow from 560 million in 2010 to 2.1 billion in 2015* and average mobile broadband network connection speeds expected to grow from 1 Mbs in 2010 to 5 Mbs in 2015**, Xilinx’s LogiCORE IP cores will help overcome higher system bandwidth requirement challenges and enable lower cost, flexibility, and a higher level of integration.

Connectivity IP cores enabling next-gen wireless infrastructure

The Serial RapidIO Gen 2 v1.2 Endpoint LogiCORE IP is designed to the RapidIO Trade Association’s RapidIO Gen 2.2 specification and is the industry’s first true Gen 2.2 soft IP core supporting line rates of up to 6.25G in 1x/2x/4x lane widths. Comprised of a highly flexible and optimized Serial RapidIO Physical Layer core and a Logical (I/O) and Transport layer core, this IP core is supported by 7 series and Virtex®-6 FPGAs and comes with a configurable buffer design, reference clock module, reset module, and configuration fabric reference design that allows flexibility in selection of functional blocks needed for a given application. The IP core also doubles the data bandwidth in FPGA/CPU/DSP multi-processor farms to implement complex algorithmic and signal processing functions in systems such as wireless infrastructure to accommodate ever increasing system data throughput.

The CPRI v4.1 LogiCORE IP is designed to the Common Public Radio Interface (CPRI) standard specification v4.2 and is ideal for connectivity between Radio Equipment Controllers (REC) or baseband/channel cards and one or more Radio Equipment units (radio cards). With distributed base stations and cloud based RAN concepts moving radios closer to the users for optimal capacity and coverage, the CPRI protocol enables distributed base stations by deploying radio heads remotely. The IP core provides an optimized implementation supporting radio I/Q data, radio unit management, and synchronization in a single efficient protocol. Supported by 7 series FPGAs, Xilinx CPRI v4.1 LogiCORE IP doubles the connectivity to the remote radio heads to 9.8G to enhance system data capacity.

As data converters sample rates are rapidly increasing to support increasing system data throughput, the Xilinx JESD204B v.1.1 LogiCORE IP replaces wide parallel interface to data
converters with 1/2/4 high speed serial interface links to overcome I/O constraints and PCB layout cost and complexity. The JESD204 v1.1 LogiCORE IP is the industry’s first soft IP core that is designed to Joint Electron Devices Engineering Council (JEDEC) JESD204B standard, which describes serial data interface and the link protocol between data converters and logic devices. Supported by 7 series FPGAs, this IP core can be configured as JESD204B Transmitter for interfacing to DAC device or JESD204B Receiver for interfacing to ADC device.

**Pricing and availability**
The Serial RapidIO Gen 2 v1.2, CPRI v4.1, and JESD204B v1.1 LogiCORE IP cores are available in Xilinx’s ISE Design Suite 13.3 and can be evaluated free of charge. For more information, contact a local Xilinx sales representative or go to [www.xilinx.com/ise](http://www.xilinx.com/ise).

*Infonetics (September 2011)*

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