You normally use TDR (time-domain reflectometry) to measure impedance change along a signal path (Reference 1). It is also a valuable tool for measuring propagation delays. The TDR technique is applicable to any high-speed circuit. You can use the propagation delay of a high-speed pin-electronics IC in ATE (automatic test equipment) to perform these measurements. These ICs contain high-speed drivers, active loads, and window comparators that operate in excess of 1 Gbps.

To perform TDR, you propagate a fast edge down a signal path and observe the reflection. The reflection shows the impedance along that signal path, as well as the delay that each change in the impedance imposes (Reference 1). In this case, the $T_{DLY}$ is the delay of the PCB (printed-circuit board) run you are measuring, and $Z_0$ is the impedance of the PCB run. Using TDR eliminates direct probing of the circuit, which is a difficult procedure because it entails placing probes on the device pins. These probes become part of the high-speed signal path and distort the signal you want to measure. Even a high-impedance active probe can load your circuit.

Rather than using active probes, you can use the TDR measurement capabilities of a Tektronix TDS8000-series oscilloscope with a model 80E04 TDR sampling module (Reference 1).
The sampling heads have a 20-GHz bandwidth. You also use an Agilent/HP 8082A pulse generator. You can use an evaluation board from the IC manufacturer for the DUT (device under test).

Using this setup, you make several measurements. You measure the delay due to the SMA (subminiature Type A) connectors J14 and J13 and the PCB runs under the heat sink. You measure the delay from the output of the IC through SMA connector J18. You measure the delay in the test cable connecting the DUT1 output to the oscilloscope. You measure the total delay from the DATA1 and NDATA1 inputs to the DUT1 output and through the cable to the oscilloscope. The data from these measurements let you calculate the signal delay through the IC.

Because TDR responses can be confusing, you should model the input delays using a Spice simulator.
You compare the simulation with actual measurements and model the DATA1 and NDATA1 PCB runs as 6-in. lengths with 65\(\Omega\) impedances. These traces are intended to be 50\(\Omega\) runs, but TDR measurements show them to be 63\(\Omega\). You terminate the NDATA1 output to ground. Because DATA1 and NDATA1 are symmetrical, with identical lengths to the pins of the IC, you need to measure only the DATA1 PCB run. You also model a 12-in. cable from the generator, although that model is not necessary for the actual propagation-delay measurement. You solve the Spice simulation for the voltage at test point TPv3. The simulation input signal is a step function with a 0.5V amplitude. This amplitude emulates the TDR signal from the oscilloscope. You can read the time delays for various elements in the model directly from the horizontal axis.
The part of the waveform labeled Step 1 represents the 12-in. cable from the pulse generator. The simulated delay time is about 3 nsec—twice the actual delay of 1.5 nsec. The part of the waveform labeled Step 2 represents the delay for the DATA1 PCB run. The simulation shows a delay of approximately 2 nsec—twice the actual PCB delay of 1 nsec. The other delays represent reflections of the pulse through the DATA1 PCB run.

The impedance of these various elements is proportional to voltage, as the Y axis indicates. The X axis represents signal reflections due to the single-input step signal directly in time. You can compare this simulation with the ideal version of this signal (Figure 1).

Use the following procedure to measure the propagation delay through the IC. First, measure the delay of the 2-in. SMA cable that attaches the DUT1 node to the oscilloscope’s vertical input (Figure 6). Connect the 2-in. SMA-SMA cable to one input of the TDR module, leaving the other end open. You make the measurement using the TDR pulldown menu. Note that the waveform looks like the “open” example in
Because the 804-psec delay is twice the delay of the cable, the equivalent “cable length” is 402 psec. Also note that the second waveform step is exactly halfway between the top and bottom steps. Recalling the TDR basics, this fact indicates that the impedance of this 2-in. cable is truly 50Ω.

You next measure the delay and impedance of the PCB run associated with the DATA1 input signal. You should verify the accuracy of the model by comparing this waveform with the simulation of
You set the cursors to measure the impedance of the trace. The first waveform step is 50Ω, representing the cable from the oscilloscope. The second cursor shows an impedance of 97.8Ω, representing the value of the IC’s internal 100Ω resistor that connects across DATA1 and NDATA1, which RL1 represents. The impedance of the second waveform step measures 63Ω, meaning that the PCB runs for DATA1 and NDATA1 were not designed to be 50Ω, as you would expect. The 150Ω level for the third reflection represents the sum of delays for the 50Ω cable and the 100Ω resistor.

To make this measurement, connect one end of the 12-in. SMA cable to the oscilloscope and the other end to the DATA1 SMA input connector on the evaluation board. You should ground the NDATA1 SMA connector with an SMA ground, as
The SMA cable should be as short as possible, but its length is irrelevant to the propagation-delay measurement.

You need not apply power to the evaluation board. The measurement was made with the IC soldered onto the board and no power applied. Some users prefer to make this measurement without soldering the device. Disconnecting the IC simulates an open condition, as shows. The SMA cable should be as short as possible, but its length is irrelevant to the propagation-delay measurement.

The first waveform step corresponds to cable delay, which is not of interest. The second waveform step represents the delay of the DATA1 PCB run (
The DATA1 PCB delay is 0.695 nsec—half the second-step measurement of 1.39 nsec. This result is larger than the model predicts, but the model estimate is only for comparison purposes.

You make measurements between dips in the signal. These dips indicate the presence of distributed capacitance, which the SMA connector on the board and the DATA1 pin of the IC create. As a consequence, you measure between the dips to ensure that the measurement includes SMA and pin delays. The inductance of the SMA connection to the board creates a waveform bump. You take the measurement before this bump to ensure that you capture the full board delay.

Next, you measure delay and impedance for the PCB run that connects to the DUT1’s output signal.
Figure 9: You measure delay and impedance for the PCB run that connects to the DUT1’s output signal.

Figure 7: You measure the delay and impedance of the PCB run associated with the DATA1 input signal.

). Use the same setup as
You connect a 2-in. SMA cable between the TDS8000 80E04 module and the DUT1 SMA connector on the MAX9979 evaluation kit. The first waveform step represents the 2-in. cable. The TDR’s signal amplitude is 0.5V. The 250-mV amplitude indicates that the cable impedance is 50Ω.

You make the DUT1 delay measurement between the two dips, just as with the DATA1 measurement. The level between the dips is 50Ω, indicating that the short PCB-metal run to DUT1 is close to ideal. It’s difficult to measure the PCB delay for DUT1 because its impedance appears the same as that of the cable. If the IC were not soldered to the board, you would see the three-step signal, indicating an open. You can still measure this delay with the IC soldered in place. An examination of the capacitive dips reveals one dip corresponding to the SMA connector, soldered to the board, and one dip corresponding to the IC’s DUT1 pin. You should look for an inductive bump corresponding to the SMA connector. Ensure that this bump is between the two capacitive dips. The delay is 360 psec. You halve this value to obtain the actual DUT1 PCB delay of 180 psec.

The impedance of the DATA1 run is 63Ω. The DUT1 node has an impedance of 50Ω. Ideally, these impedances should be the same, meaning that the metal on the DATA1 inputs is narrower than that of the DUT1 output.

You should set up the differential signal generator with two identical SMA cables. You then measure the baseline delay on the oscilloscope. C1 and C2 represent the complementary-PECL (positive-emitter-coupled-logic) DATA1 and NDATA1 signals.
Waveform M1 is a mathematical calculation of the differential signal between C1 and C2. Its amplitude is 900 mV, and its rise and fall times are each 700 psec. These characteristics indicate that you have acquired a valid set of data. You then trigger the scope and measure one of M1’s zero-crossing points as 29.56 nsec. Power up the IC and measure the same crossing point as it is delayed through the evaluation board. This delay includes the delay of the two input cables. These delays cancel out because you use the same cables to measure signal delay through the PCB. Keep these cables short, but their delays are not important for the propagation-delay measurement.

Figure 10 C1 and C2 represent the complementary-PECL DATA1 and NDATA1 signals. 

) with an amplitude of 450 mV. You feed the signals to the inputs of the oscilloscope from the external generator.

Using the two cables from the setup, connect the DATA1 and NDATA1 signals to the board’s DATA1 and NDATA1 inputs. The oscilloscope setup and the trigger are the same as they were previously. Refer to the evaluation board’s documentation to set the IC for signal amplitudes of 0 to 3V. The output of the board terminates in 50Ω because that is the input impedance of the oscilloscope. The 50Ω load halves the output signal, producing an amplitude of 0 to 1.5V (
You can verify that the rise and fall times are well within the IC’s specifications, meaning that clean and valid DATA1/NDATA1 signals are driving a clean and valid output. You can measure the zero-crossing point as 33.77 nsec.

You can now calculate the IC’s propagation delay. The total delay through the evaluation board is 33.77 nsec–29.56 nsec=4.21 nsec. You then subtract the PCB-trace delay of DATA1 from the total delay to get 3.515 nsec. Subtract the DUT1 PCB-run delay of 0.18 nsec, which yields 3.335 nsec. Finally, subtract the delay of the 2-in. cable to the oscilloscope for a result of 2.933 nsec. This result correlates well with the IC data sheet’s specification of 2.9 nsec for a typical delay.

Using TDR for measuring propagation delays has several advantages. It gives accurate measurements; requires no active probes, thus avoiding the inaccuracies they introduce; and is a simple technique that suffices for most propagation measurements. The measurement also lets you check for correct impedances on connectors and PCB runs. The TDR signals reveal excess capacitance and inductance in the signal path should you need to redesign the board. You can verify the TDR measurement with simple modeling and simulation tools.

As signal speeds rise, the errors and mistakes of timing measurements can cause incorrect planning decisions, faulty device selections, and bad system design. The use of best practices in high-speed measurements is always a good idea.

Reference