Capacitance meter uses PLL for high accuracy

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An old *Electronics Designer’s Casebook* described a circuit that provided capacitance measurements of 10 pF to 1 µF with 1% accuracy ([Reference 1](#)). A number of issues emerged with the circuit during testing, and this Design Idea describes an improved circuit. The meter circuit in **Figure 1** lets you measure capacitance from 10 pF to 10 µF with high accuracy. It needs no microprocessor; thus, it needs no code. Even in the 1- to 10-pF range, the circuit is accurate to about ±1 pF when reading values as low as 5 pF.

![Figure 1 A capacitance meter connects to a frequency counter measuring pulse width to provide a capacitance measurement.](#)

The circuit requires a high-input-impedance device to interface with the high-value resistors, $R_6$, $R_8$, $R_9$, and $R_{10}$, and a fast comparator to interface with the PLL (phase-locked loop). IC$_1$, an [Analog Devices](#) AD8033 op amp, does the job because of its 1000-GΩ input impedance and 1.7-pF input
capacitance. It also has only 50 pA of input bias current over temperature. Its 80-MHz bandwidth and 80V/µsec slew rate are more than enough for this application. It can operate with just an 8V power supply. Unfortunately, the AD8033 is available only in surface-mount packages, which makes breadboarding somewhat tedious. IC₂, an Analog Devices ADCMP601 comparator, interfaces with the AD8033 op amp and IC₃, a 74HC4606A PLL. The comparator has a typical propagation delay of only 4.3 nsec. It has built-in hysteresis and needs only a 5V supply. It is also available only in surface-mount packages.

The capacitance meter generates two signals; one of them lags the other by 60°. A 3-bit, self-correcting, divide-by-six twisted-ring counter comprising IC₆, IC₇, and IC₁₃B provides the lagging signal. The lagging signal connects to the COMP input of the PLL (Pin 3), and the other signal is applied to an RC circuit, which provides a 60° phase lag before it gets to the SIG input of the PLL (Pin 14). The PLL adjusts the frequency of its VCO (voltage-controlled oscillator) so that the two input signals are in phase. The resulting period of the VCO’s output signal (Pin 4) is proportional to the measured capacitance.

On the low-capacitance range, signals with frequency \( F_0 \) are applied to the PLL. On the high-capacitance range, the frequency is \( F_0/1000 \). IC₈ through IC₁₀ provide the division, and S₂, IC₄B through IC₄D, IC₅D, IC₅E, and the associated components provide the high-capacitance/low-capacitance range switching. The VCO of the PLL runs at 6\( F_0 \). The circuit divides this signal by three to provide an output with a period that’s proportional to the measured capacitance. It provides the correct digits when you measure with a frequency counter that you set to measure the period. You can calculate \( F_0 \) or \( F_0/1000 \) from \( 0.1505/R_XC_X \), where \( R_X \) is \( R_6, R_8, R_9 \), or \( R_{10} \), depending on the selected range.

The 74HC4046A PLL can exhibit several problems. For example, it may not start when you apply power, or it may hang with the VCO running with the VCO-input pin (Pin 9) stuck high or low. The start-up circuitry, comprising IC₁₃F, Q₄, and associated components, applies a positive voltage of approximately 2V to the VCO’s input, which forces the VCO to oscillate. After the VCO starts, D₄ becomes back-biased, which disconnects the start-up circuitry from the VCO’s input pin. If the VCO is running but hung with its input stuck high or low, one-shot IC₁₂A detects that it’s not phase-locked by responding to pulses from Pin 1 of IC₃. The one-shot then issues a 1.5-sec pulse that causes IC₁₂B to produce a 0.5-sec pulse that causes either a positive pulse at the inhibit pin or a low pulse at the VCO’s input pin, depending upon whether the PLL is low or high. After the 0.5-sec pulse ends, the pulse from IC₁₂A continues for 1 sec, giving the PLL time to lock. LED D₇ indicates phase lock. If the PLL phase locks, all is well. If it does not, the IC₁₂A/IC₁₂B one-shots continue issuing pulses. Experiments determined these methods for recovering from the anomalous states. It’s possible that the circuit won’t always recover, but these methods have been effective on the test unit.

The circuit applies the 6\( F_0 \) signal, divided by three, to buffer IC₅F’s Pin 5. This action provides an output frequency whose period is proportional to the value of the measured capacitance. The output provides the correct digits without regard to the location of the decimal point. To determine the value of the unknown capacitance, observe the setting of S₁ and S₂.

You can calibrate the circuit by using a capacitance of a known value of approximately 1000 pF, with S₂ at the low-capacitance position and S₁ at the 100- to 1000-pF/0.1- to 1-µF position. Set R₂₂ at its midposition, connect a frequency counter to Pin 6 of IC₅F, and set the meter to measure the period of the signal. Adjust R₁₂ for a period whose digits agree with the known value of capacitance. Next, use
a capacitance of approximately 100 pF and set S₁ to the 10- to 100-pF/0.01- to 0.1-µF position. Record the measured value of the capacitor. Then, using the same capacitance of approximately 100 pF, set S₁ to the 100- to 1000-pF/0.1- to 1-µF position and adjust R₂₂ to get the same value as you obtained on the 10- to 100-pF/0.01- to 0.1-µF position. The R₅/C₁₃ combination provides a small variable delay relative to the signal at Pin 14 of IC₃. This fine adjustment improves accuracy in the lower range.

Employing measurements made with the available equipment, which did not include an accurate, high-resolution capacitance meter, this meter is accurate to approximately ±2% over 100 pF to 10 µF (Table 1). The accuracy degrades over 10 to 100 pF because of the input capacitance of the op amp and the associated parasitic capacitance at IC₁’s Pin 3. R₅ and C₆ provide some compensation at the 10- to 100-pF range for the inherent capacitance at that node. R₃ and C₃ provide compensation at the 1- to 10-pF range.

<table>
<thead>
<tr>
<th>TABLE 1 CAPACITANCE MEASUREMENTS</th>
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<tbody>
<tr>
<td>Range</td>
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<tr>
<td>Capacitance</td>
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<tr>
<td>Measurement error (%)</td>
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You can also measure the inherent capacitance and then subtract it from the reading on the two lower ranges. If you take this approach, omit R₅, R₃, C₅, and C₆ from the circuit. Then, with S₁ at the 1- to 10-pF range and S₂ at the low-capacitance position, you can measure the capacitance at that node with no external capacitance. The intrinsic capacitance of the test circuit is 2.8 pF. Using this correction, the values you obtain on the lowest two ranges are accurate to approximately ±2%, or ±1 pF.

You must observe capacitor polarity when measuring electrolytic capacitors. Connect the negative end of the capacitor to the grounded terminal. Also, the circuit provides no overvoltage or ESD (electrostatic-discharge) protection, so be sure to discharge the capacitors before connecting them to the capacitance meter and use an ESD wrist strap to avoid damaging the circuit. For best results, you need accurate and stable 5 and 8V power supplies. Both supplies should be accurate to ±2%. You can raise the 8V supply to 9V and relax the accuracy to 5%. If you use a 9V battery to supply the 8V, you can let the voltage drop to about 7.9V before adversely affecting the performance of the meter. You must, however, maintain the 5V supply at a constant, accurate value. Note that all of the ICs except IC₁ have 0.1-µF bypass capacitors from their 5V pins to ground.

**Reference**