Preamplifier and read-channel design addresses hard-drive goals

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As the capacity of hard-disk drives continues to increase, the burden on the system to reliably access data on the media also increases. For read accesses in particular, this challenge is creating the need for ever-more-complex signal-conditioning and -processing algorithms to recover the data from the ever-decreasing signal quality—that is, lower SNR (signal-to-noise ratio)—of information coming off the media. To make the situation even more challenging, price, power consumption, and speed trends are all moving in difficult-to-address directions. Cost and energy draw must continue to decrease, and the rate at which the data comes off the disk must increase from one generation to the next. All of these factors make for a difficult but rewarding design challenge.

Technology overview

Before delving into the benefits of jointly designing the preamplifiers and read channels, you should briefly consider the functions of each block. The preamplifier resides between the read head, which senses the bits on the disk, and the read channel (Figure 1). A primary function of the preamplifier is to faithfully transmit the noisy signal from the head to the read channel with minimal distortion and other degradations. The preamplifier accomplishes this objective by first amplifying the head signal and then driving it to the read channel (Figure 2).

The first function of the read channel is to further condition the partially processed signal from the preamplifier through a series of filters and gain stages (Figure 3). From there, the conditioned signal goes to the signal-processing section for conversion into a faithful representation of the original digital data that was previously written on the disk.

The signal-processing section typically comprises a detector, an inner code, and an outer code (Figure 4). The signal-processing function block implements complex algorithms that have evolved over time from a simple peak-detection system to a full-blown LDPC (low-density-parity-check) system in migrating toward the Shannon capacity limit (Figure 5).

System optimization

To achieve an optimal result, engineers must model, simulate, and design the datapath from the head to the output of the read channel as a system, not simply as a series of independent blocks. A system-design approach allows you to make the proper trade-offs with respect to performance, power, and cost. The signal coming from the media must travel though a complicated path before it becomes valid data at the output of the read channel. It flows through the head, down a flexible transmission wire, into the preamplifier for boosting and filtering, down another flexible
transmission wire, and then into the read channel's signal-conditioning block, where it is further amplified, filtered, and linearized.

Each of these interfaces requires proper design to ensure optimization of the signal bandwidth, dynamic range, termination impedances, and transmission effects. Failure to fine-tune the signal-conditioning path will lead to suboptimal performance for which the read channel's signal-processing block may be unable to compensate.

Because both the preamplifier and the read channel bear the signal-conditioning burden, the trade-offs you make in these areas can both optimize performance and lower the overall system power consumption and cost. Manufacturers typically build the read channel in a fine-line CMOS process for large digital circuits that use low-voltage power supplies. Therefore, you decrease power consumption and cost in the silicon area when you minimize the number of pure analog circuits you use in favor of digital signal conditioning and digitally assisted analog circuits. These circuits can then run on the core transistor's power supply—typically at 1V—instead of the I/O's power supply, which is typically 2.5V.

Digitally assisted analog circuits can, for example, comprise DACs to set up the gain in a variable-gain amplifier (Figure 6). They can also find use in setting the pole frequency in a lowpass filter instead of relying on the traditional variable-resistor analog-feedback technique. Small, low-power DACs can also zero out offsets, allowing the use of high-speed and low-power core transistors.

Manufacturers usually build preamplifiers in an older, less-expensive bipolar or Bi-CMOS process for analog performance using higher-voltage power supplies. Pure analog amplifiers and filters are therefore efficient; digital signal-conditioning circuits, however, are not. The logic in a preamplifier process is typically lower-performing and runs from a higher-power supply. Therefore, it is critical to properly divide the signal-conditioning task between the preamplifier and the read channel.

Another benefit of designing the preamplifier and read channel together is that you can save power by taking advantage of your knowledge of mode transitions that pass between the blocks. This premonition allows for the activation or shutdown of function blocks at precise times to ensure that circuits power up only when absolutely necessary. With previous implementations, function blocks would remain in a high-power state because they would not know when the next command was coming. They could not enter into a low-power state because the transition back to fully on mode would take too long to settle out. However, advance knowledge means that it is no longer necessary for circuitry to perpetually remain in a high-power state. It can power down and then later move back to fully on mode through an early wake-up signal. The end result is a system with a lower power draw, an important feature for hard-disk drives.

You can achieve further system-performance improvements by minimizing the distance between the head and the data on the media (Figure 7). The lower the head flies over the media, the stronger the signal becomes, thereby improving the SNR. Therefore, a control loop at a good flying height between the head, the preamplifier, and the read channel is critically important. You must provide compensation within the signal-processing block for the nonidealities of signal-conditioning circuits to control the flying height of the head.

In the near future, the media will evolve from a continuous magnetic plane into patterned media in which each bit is physically isolated from others. This transition will greatly complicate the writing of the data to the media because it will require precise control of the time that the data writes to the bit cell. You must comprehend and compensate for delay variations with respect to environment, voltage, and process. You can accomplish this objective only by using a well-controlled feedback loop, in which you design the preamplifier and the read channel.