Understanding power-over-Ethernet power allocation

Daniel Feldman - August 10, 2009

It’s time to bust some myths about POE (power-over-Ethernet) power management and allocation. First, there are those who erroneously believe that POE switches and/or midspans with a power supply smaller than 15.4W per port should allocate power based on a PD’s (powered device’s) IEEE classification. This, unfortunately, only enables static power management, since not all PDs support classification and the system defaults to full 15.4W of power allocation, quickly consuming available power budget. A second fallacy, which has emerged with the advent of high-power IEEE 802.3at standards, is that network administrators must rely on worst-case power budgets that account for a full 25.5W per PD and 4.5W of cable loss, since some claim that few systems can determine the PD’s power usage and cable losses.

The truth: Today’s POE silicon has given POE midspans and switches a variety of advanced capabilities for smart power management by leveraging an important new POE distributed power architecture. This architecture optimizes energy efficiency and accommodates the latest high-power IEEE 802.3at requirements.

Read more Guest Opinions

It’s important to understand POE history. Earlier IEEE 802.3af-compliant PSEs typically delivered full power per port (with or without redundancy), but with less than full power per port in most systems. This created a substantial energy drain since large POE supplies dissipate power even when not fully utilized. For instance, in a typical 48-port switch with 800W of full power per port, only 20 ports might be used at any given time. This wastes up to 80W of quiescent power. Also, while there are IEEE 802.3af applications that could require full power per port, IEEE 802.3at applications don’t normally require full power on any single port, and definitely are less sparse than IEEE 802.3af applications. Plus, in many cases, IEEE 802.3at PSEs are powering IEEE 802.3af devices, further complicating the power-management and -allocation picture.

These challenges are solved by replacing the earlier large power supply with a smaller, more economical internal default power supply that is supplemented by external power supplies for incremental additional power as required. The resulting distributed power architecture improves overall system efficiency, facilitates prioritized per-port backup power, reduces heat dissipation, and minimizes costs since the smaller, more economical power supplies require smaller and/or lower-speed fans.

A number of silicon advances were needed in order for the industry to deploy this new distributed power architecture. The architecture requires SOC (system-on-chip) ICs with low power dissipation,
very fast reaction times for managing the overall power budget, and highly accurate power allocation.

The next generation of smart POE PSE ICs has been built with the dynamics of power dissipation and management in mind. Earlier POE PSE ICs built for IEEE 802.3af had 2Ω of Rsense and 0.5Ω of $R_{DSon}$ (FET), resulting in 0.3W/port of dissipation in dc disconnect on the resistors and FETs. In contrast, the latest smart POE PSE ICs have much lower sense resistors (0.5Ω) and also have external (or very-low-resistance internal) FETs (0.1Ω). This cuts power dissipation to 0.07W/port in IEEE 802.3af mode or 0.22W/port in IEEE 802.3at mode for dc disconnect (where supported).

Today’s POE silicon also can allocate power either dynamically (that is, according to the power consumed by the device) or in a static or pseudostatic fashion, with the device and PSE communicating via hardware classification or the new Layer 2 classification of IEEE 802.3at-draft 4.2. As mentioned earlier, the IEEE 802.3af standards may support the latter approach, but most PDs do not support it and therefore default to full 15.4W power allocation from the PSE to the port. This quickly consumes available power budget. Further, the classifications are so broad that, when a PSE detects a higher class, it delivers the full incremental additional power, rather than just what’s needed by the device.

Dynamic power management is the better approach. It enables real-time measurement and management of power on each port. This eliminates the need for fixed power allocations, since only the necessary power is delivered to each port. The system monitors the actual per-port power consumption, including what is consumed by Class 0 PDs (which would otherwise always be delivered full power).

In practice, the process is quite simple. There is no need to know PD power classifications or determine how to allocate power per port or across the network. As an example, Microsemi’s PowerDsine midspans eliminate the need for preallocation of power or a fixed denomination of ports. The benefit of this approach is significantly improved overall system power efficiency. In the case of a typical 1U 24-port midspan, there might typically be 24 x 15.4W, or 370W, of power to manage, but the various network PDs might need only half that in real time. By using dynamic power allocation and a distributed power architecture, the PowerDsine midspan needs only a 200W supply to support real-time network power demand, and uses external power supplies for incremental additional power as needed. Multiple dc input power sources provide additional power to a lower internal power supply, and the midspan is able to discern, in real time, that an external power source has been changed or disconnected. This eliminates the possibility of a failure on all ports, or a switch power supply failure leading to a switch reset. The midspan is able to respond to the situation and ensure that the higher-priority ports remain operational.

POE technology offers a variety of increasingly important capabilities. Thanks to key system and silicon advances, today’s midspans and switches have all the information they need to intelligently and cost-effectively allocate and manage power using dynamic power management.

**Author Information**

_Daniel Feldman is director, telecom products, for Microsemi Corp’s Analog Mixed Signal Group._