Advantages of interleaved boost converters for PFC

Michael O'Loughlin - March 30, 2006

The most popular topology for PFC (power-factor-corrected) preregulators is the boost converter, which has continuous input current that you can manipulate with average-current-mode-control techniques to force input current to track changes in line voltage. Figure 1 shows a traditional single-stage boost. (To more easily explain the circuit operation, this article refers to dc inputs.) The change in inductor ripple current, \( \Delta I_L \), is directly at the converter's input and may require filtering to meet EMI specifications. The diode output current, \( I \), is discontinuous and requires the output capacitor, \( C_{OUT} \), to filter it. In this topology, the output-capacitor ripple current, \( I_{COUT} \), is high and is the difference between \( I \) and the dc output current, \( I_{OUT} \).

Interleaving boost converters

Figure 2 shows the functional diagram of a two-phase interleaved boost converter, which comprises two boost converters operating 180° out of phase. The input current is the sum of the two inductor currents, \( I_{L1} \) and \( I_{L2} \). Because the inductor's ripple currents are out of phase, they cancel each other out and reduce the input-ripple current that the boost inductors cause. The best input-inductor-ripple-current cancellation occurs at 50% duty cycle. The output-capacitor current is the sum of the two diode currents, \( I_1 + I_2 \), minus the dc-output current, which reduces the output-capacitor ripple, \( I_{OUT} \), as a function of duty cycle. As the duty cycle approaches 0, 50, and 100%, the sum of the two diode currents approaches dc. At this point, the output capacitor has to filter only the inductor-ripple current.

Input-ripple-current reduction

The following equations and Figure 3 show how the ratio of input-ripple current to inductor-ripple current, \( K(D) \), varies with changes in duty cycle. It is important to remember this variance when selecting inductors for the interleaved boost converter.

\[
K(D) = \frac{\Delta I_{IN}}{\Delta I_L}.
\]

If \( D \leq 0.5 \), then:

\[
K(D) = \frac{1-2D}{1-D}.
\]

If \( D > 0.5 \), then:

\[
K(D) = \frac{1-2(1-D)}{1-(1-D)}.
\]

Figure 4 shows the normalized output capacitor rms current in a single-stage boost converter, \( I_{COUT_{rms\_single}}(D) \), and the normalized rms current in a two-stage interleaved boost converter, \( I_{COUT_{rms}}(D) \), as a function of duty cycle. The figure demonstrates that the output-capacitor-ripple
current in a two-phase interleaved boost converter is roughly half that of a traditional single-stage boost converter, reducing the electrical stress on the output-filter capacitor.

$$I_{\text{OUT RMS SINGLE}}(D) = \sqrt{1-D \times [1-D]}.$$  
$$I_{\text{OUT RMS}}(D) = \sqrt{{\frac{1}{2}} (1-D) \times [1-2(1-D)]} \text{ IF } D > 0.5.$$  
$$I_{\text{OUT RMS}}(D) = \sqrt{{\frac{1}{2}} [2(1-D)-0.5] \times [1-2(1-D)-0.5]} \text{ IF } D < 0.5.$$  

**Evaluating inductor size**

To evaluate the benefits of interleaving PFC preregulators' reduced boost-inductor size, I conducted a mathematical comparison between a single-stage and a two-phase boost preregulator (Figure 5). The design requirements were a maximum output power, $P_{\text{OUT}}$, of roughly 350W; a minimum line input, $V_{\text{INMIN}}$, of 85V rms; a maximum line input of 265V rms; and an estimated converter efficiency of 95%. The inductors have a switching frequency, $f_s$, of 100 kHz. The inductors have an input-ripple-current requirement of 30%, and the inductors of both topologies have the highest inductor-ripple currents that occur at the minimum input and maximum input current.

I selected the inductors for both designs based on the worst-case ripple current. For a converter for a universal input, this point occurs at the minimum input at the peak line voltage, with the converter operating at a minimum duty cycle of 0.67. Figure 6 shows how the duty cycle varies with line voltage $V_{\text{IN}}(t)$. Function $D_1(t)$ shows how the duty cycle varies with changes in line when the input is at 85V rms. Function $D_2(t)$ shows how the duty cycle varies with a maximum input of 265V rms. When the converter is operating at a maximum input of 265V rms, the maximum inductor-ripple current occurs when the input voltage is at half the output voltage. As the line voltage approaches the output voltage, the duty cycle decreases, reducing the inductor-ripple current.

The inductor-ripple current in a single-stage PFC preregulator is evident at the converter’s input. A single-stage PFC inductor for a universal input would be roughly 450 $\mu$H. I based this calculation on where the inductor-ripple current was greatest at 85V rms input and 0.67 minimum duty cycle.

$$L_{\text{SINGLE}} = \frac{V_{\text{IN MIN}} \sqrt{2} \times D \times f_s}{V_{\text{OUT}} \sqrt{2} \times 0.3 \times 0.3} \approx 450 \mu H.$$  

The dual-interleaved inductor has the same input-current-ripple requirements as the traditional preregulator. The change in inductor current in one of the interleaved boost stages is roughly 3.4A. Variable minimum duty cycle at the minimum rms input voltage requires an inductance of roughly 245 $\mu$H—about half the inductance a single-stage PFC preregulator at the same power level requires.

$$\frac{P_{\text{OUT}} \sqrt{2} \times 0.3}{V_{\text{IN MIN}} \times 0.95} \approx 34 \text{A}.$$  
$$\Delta L_1 = \frac{V_{\text{IN MIN}} \times 0.95}{K(C_{\text{MAX LL}})} \approx 34 \text{A}.$$  
$$L_1 = \frac{V_{\text{IN MIN}} \times \sqrt{2} \times D_{\text{MAX LL}}}{\Delta L \times f_s} \approx 245 \mu H.$$  

**Lab results**
I evaluated a dual-interleaved boost converter using 200-µH inductors for L₁ and L₂ and the input current. The worst-case inductor-ripple current occurs when the converter operates at low input at the peak of the line. The oscilloscope plot in Figure 7 shows the inductor currents of L₁ and L₂ with an input of 85V rms. CH₁ is the rectified line voltage, CH₂ is L₁ inductor current, CH₃ is L₂ inductor current, and CH₄ is input current. The current-conversion ratio is roughly 4A/division.

Figure 8a and Figure 8b show the input-line and inductor-ripple currents at maximum load. The channels of the scope plots are the same as in Figure 7. These waveforms clearly demonstrate a clean input-current waveform for Channel 4. This two-phase, interleaved-PFC design uses a 220-µF output capacitor. At full load for a single-stage, 350W PFC preregulator, the output-capacitor ripple would be roughly 33.5V. For a two-phase, interleaved PFC, the output ripple should be less than half of the single stage. The prototype's output-ripple voltage at full load is roughly 13V (Figure 9).

$$V_{\text{Ripple}} = \left( \frac{P_{\text{OUT}}}{V_{\text{IN,MIN}} \times 0.535} \right) \times \frac{1}{2 \pi f L \text{OUT}} \approx 33.5V.$$ 

Determining whether the prototype could meet current harmonic specifications EN61000-3-2 requires the prototype's input harmonics' full-load power. The first harmonic is the rms input current at 60 Hz. The proceeding harmonics are well within CH61000-3-2 Class D specifications (Figure 10).

Interleaving PFC preregulators allows power-supply designers to reduce inductor magnetic volume. The inductor-ripple-current cancellation at the input of the power converter allows designers to reduce the inductance by roughly half. Interleaving also reduces the ripple current in the boost capacitor, alleviating electrical overstress on the output capacitor. With no filtering on the prototype circuit, the design achieves EN61000-3-2 Class D current-harmonic specifications. It has a slightly more complicated control scheme with a higher component count, but, in high-power applications, this trade-off is well worth it.