Cores lower entry cost for custom SOCs

Robert Cravotta - March 08, 2006

Tensilica based its new Diamond Standard family of six processor configurations on the Xtensa architecture. Each core implements the Xtensa instruction-set architecture in a five-stage-pipeline, 32-bit architecture. The cores support modeless switching between 16- and 24-bit instructions to deliver high code density, high processing performance, and low power consumption. These processors offer a lower price to design teams considering the Tensilica technology.

The family comprises the 108Mini, a cacheless RISC controller processor, which can deliver lower power consumption than ARM7-based approaches. The smallest device in the family, the 108 Mini uses a 0.38-mm² cell area in a 0.13-micron process and consumes 0.06 mW/MHz with the 0.13LV libraries or 0.09-mW/MHz with the 0.13G libraries.

The low-power, 24-bit Diamond 330HiFi audio processor supports audio and speech codecs; Tensilica based it on the Xtensa HiFi 2 Audio Engine. It supports decoding and encoding for Dolby Digital AC-3, MP3, aacPlus, and WMA; SBR (spectral-band replication); parametric stereo; QSound MIDI; 3-D audio; and G723-1 and G729AB VOIP (voice-over-Internet Protocol) codecs. The midrange Diamond 212GP RISC controller offers DSP support, including 16 multiply/accumulates, 16 multipliers, minimum/maximum, clamps, sign extend, and NSA instructions. It includes instruction and data caches, as well as user-selectable local-memory sizes, and it competes with ARM9-based approaches for better processing performance and lower power consumption. It uses a 0.58-mm² cell area in a 0.13-micron process and consumes 0.085 mW/MHz with the 0.13LV libraries or 0.135 mW/MHz with the 0.13G libraries.

The midrange Diamond 232L RISC-processor core includes a full MMU (memory-management unit) to support the requirements of the Linux operating system. It includes the same DSP support as the 212GP. The core requires a 0.71-mm² cell area in a 0.13-micron process and consumes 0.10 mW/MHz with the 0.13LV libraries or 0.145 mW/MHz with the 0.13G libraries.

The high-performance, three-issue Diamond 570T static superscalar processor core competes with the ARM1136JF-S core based on EEMBC (EDN Embedded Microprocessor Benchmark Consortium) benchmarks. The core includes both a 32-bit input and a 32-bit output queue that support direct access to data from the pipeline with no loads or stores. The core uses a 0.96-mm² cell area in a 0.13-micron process and consuming 0.11 mW/MHz with the 0.13LV libraries or 0.15 mW/MHz with the 0.13G libraries. The highest performance Diamond 545CK licensable core delivers digital-signal processing using a three-issue VLIW (very-long-instruction-word) processor containing eight MACs that support SIMD (single-instruction-multiple-data) operations. The core includes a Viterbi accelerator to support communications baseband applications.

Prices for the Diamond 108Mini is $75,000 for a single-use license with a royalty of 5 cents per core. Tensilica’s XCC optimizing compiler and Eclipse-based Xplorer IDE support software development.
on these processors with a clock-cycle-accurate, pipeline-modeled instruction-set simulator; a GNU-based tool chain, including an assembler, a debugger, a profiler, and a linker; and optimized C libraries. Operating-system support for these cores include Accelerated Technology’s Nucleus Plus, micro-Itron from Sophia Systems, Tensilica’s XTOS runtime, and open-source eCOS. Linux support for the Diamond Standard 232L is available from MontaVista’s Linux Professional.