Programmable analog circuits yield single-chip sinusoidal oscillators

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Programmable-logic devices provide a popular method of implementing complex functions in digital designs. Although manufacturers don't yet offer analog circuits whose complexity compares to VLSI digital circuits, field-programmable analog circuits are enjoying extensive use in signal-conditioning and filtering applications. Based on CMOS-operational-transconductance and switched-capacitor amplifiers, these devices offer a convenient approach to relatively complex design problems. Lattice Semiconductor's (www.latticesemi.com) ispPAC10 in-system-programmable analog circuit and its accompanying PAC Designer software offer a convenient method of circuit design and verification (Reference 1). This Design Idea presents two simple sinusoidal oscillators based on the ispPAC10.

Resistors within the ispPAC10 are fixed at a nominal 250 kΩ, and all capacitors are user-selectable from 1.07 to 61.59 pF. Figure 1 shows an ispPAC10 with its internal blocks 1, 2, and 4 connected as a cascade of three first-order lowpass filters to form a classic phase-shift RC oscillator. Altering the capacitors' values produces oscillation frequencies over a range of 18 to 130 kHz. Each PAC block's gain is fixed at a factor of two to obtain a loop gain of –8, which Barkhausen's condition for oscillation requires (Reference 2). Configured from Block 3, a first-order lowpass filter reduces the THD (total harmonic distortion) on the oscillator's output. The values of capacitors in Block 3 are optimized for filtering performance and thus differ from those of the phase-shift stages.

The circuit in Figure 2 describes a two-integrator loop that forms a classic quadrature-RC oscillator. The circuit's oscillation frequency spans 12 to 126 kHz and depends on the time constants of the integrators that blocks 1 and 2 form. In theory, each integrator's gain should have an absolute value of unity, but, in practice, ispPAC allows specification only of inverting integrators, and producing a stable sinusoidal signal requires a gain of at least –4 in Block 1. The circuit uses a gain of –10. Two additional blocks of the ispPAC10 device form a second-order lowpass filter that decreases the output's THD. In both oscillator circuits, you can alter the lowpass filters' gain so that the circuit's outputs deliver specific voltages, such as 1V p-p, at all frequencies.

Table 1 and Table 2, respectively, contain summaries of the phase-shift and quadrature oscillators' components and output characteristics. \( C_n \) refers to the value of the capacitor used in the nth PAC block for oscillation at frequency \( f_0 \). The design uses a Tektronix TDS1002 digital oscilloscope's FFT function to measure THD and the spectral line width of each output frequency at a level of –20 dB with respect to the central frequency, \( f_0 \).

Figure 3 illustrates the application of a microcontroller to dynamically reconfigure an ispPAC-based oscillator for specific frequencies. The nonvolatile memory stores frequency-specific capacitance and gain values for each of the ispPAC10's circuit blocks. Data transfers occur using the IEEE 1149.1 JTAG-standard protocol through the ispPAC10's serial test-access-port interface.
References