Minimizing power consumption has long been a major goal of many designs. The reasons range from the obvious, battery powered circuits and green systems, to the perhaps not so obvious, minimization and cost reduction in the power supply. Most designers simply look for products with the lowest power consumption specification. While a lower clock rate will generally mean lower power consumption, it is possible to reduce power consumption even more with burst-mode operation. This article describes using burst-mode operation to minimize average power consumption of ADCs (analog-to-digital converters).

All ADCs have minimum and maximum clock rates over which they can operate properly. While they are generally specified at a given sample rate, the clock rate is really the operational constraint. If the clock rate is too fast, insufficient settling of internal nodes will cause poor performance. If the clock rate is too slow, internal leakage will cause partial depletion of charge on the internal capacitors holding that charge for conversion, again resulting in poor performance.

One way to get a sample rate lower than that specified for the chosen ADC is by decimating its output. That is, use only every "nth" sample and ignore the other samples between two successive samples that are used. This can be done with any ADC, regardless of technology or architecture.

For example, the requirements of an application might require a 12-bit ADC operating at 10k samples/sec with a 3V supply. You might choose the ADC121S021 as a possibility. This device is a 12-bit, low power ADC with SPI (Serial Peripheral Interface) and is specified for operation over the power supply range of 2.7V to 5.5V and over the sample rate range of 50k samples/sec to 200k samples/sec.

Although the lowest specified sample rate for the part is 50k samples/sec, we can operate it at the 1 MHz clock rate, which corresponds to the minimum specified 50k samples/sec for this device, and then decimate the output by five, using every fifth sample. The part would essentially be powered up continually and the power consumption would be as specified for the clock rate used. In this case, the part would have a clock rate of 1 MHz, where it typically consumes just 1.5 mW with a 3V supply.

Many ADCs enter the power-down mode when deselected, as when the CS (chip select) pin is de-asserted. Running the ADC at its maximum clock
rate and shutting the device down between conversions can minimize average power consumption. This is burst-mode operation and is illustrated in Figure 1. Burst-mode operation reduces average power consumption. The peak power consumption is still the active power specified for the device.

To determine the average power consumption, take the operating or active power consumption multiplied by the percentage of time in the active mode and add to this the product of the power consumption in the power down mode multiplied by the percentage of time in the power-down mode: 

\[(\text{Active Power} \times \% \text{ active}) + (\text{PD Power} \times \% \text{ PD})\]

where PD means “power-down.”

Operating most ADCs in burst-mode will lower power consumption significantly. The only requirement for burst-mode operation is that the ADC has a power-down mode, which is true with most converters available today. It would be a great advantage if there were no delay after coming out of the power down mode before a conversion can be done and if no dummy conversions were required so that the active time (time in the active mode) can be minimized. A dummy conversion is one that is used to flush out the part after power up or after coming out of a power down mode. The results of any dummy conversion are garbage and cannot be used.

Still, there are many parts that are fully functional as soon as the command to enter the active mode is given when you bring its CS pin low and if it does not require any dummy conversions. Using this part at its minimum clock rate of 1 MHz, but using burst-mode operation rather than decimating the output, the ADC would be in its active mode 16% of the time and in power down 84% of the time. The active power consumption of the IC is 1.5 mW and power consumption in the power down mode is 0.315 mW, so the average power consumption is just \((1.5 \times 16\%) + (0.315 \times 84\%) = 0.505 \text{ mW} = 505 \mu\text{W}\). This is obviously much lower power than being in the active mode continuously, but there is room for improvement.

Operating the part at its maximum clock rate of 4 MHz (corresponding to its maximum specified 200k samples/sec) would mean the ADC would be in its active mode only 4% of the time and in power down 96% of the time for burst mode operation, for an average power consumption of \((1.5 \times 4\%) + (0.315 \times 96\%) = 0.362 \text{ mW} = 362 \mu\text{W}\). Operating an ADC at its maximum clock rate and putting it into its power down mode between conversions provides extremely low power consumption, compared with simply operating it at the desired sample rate.

If burst-mode operation provides the lowest power consumption at higher clock rates, it would seem that using a higher speed device would result in an even lower average power consumption for a given sample rate. This is indeed true. Although power consumption is generally higher in the active mode for a faster device, the converter is in the power down mode for a much longer time, resulting in lower average power consumption.

![Figure 2: Using an ADC in burst-mode can provide low-power operation that approaches the shutdown power.](image)

You can replace the previous ADC with a 1M-sample/sec one such as the ADC121S101. It is a pin and functional replacement, with a 3V power consumption of 2 mW at 20 MHz and 0.2 mW in the power-down mode. This would result in a
further reduction of average power consumption. In this case it would be active for only 0.8% of the
time and in power down for 99.2% of the time, lowering the average power consumption to just (2.0 
\times 0.8\%) + (0.2 \times 99.2\%) = 0.214 \text{ mW} = 214 \mu\text{W}. This is just marginally more power than the 200 \mu\text{W}
consumed by the device in the power down mode.

Figure 2 illustrates the power levels versus time for these conditions. In that figure we can see short bursts of power between long idle times. Table 1 summarizes the average power consumption for each of the conditions discussed here. A graph of average power consumption versus sample rate for the faster part in burst mode with 3V and 5V supplies is shown in Figure 3. Not only do we see the advantage of burst-mode operation, but we also see the intuitively obvious advantage of using a low supply voltage where practical. Burst-mode operation at very low conversion rates can provide extremely low average power consumption, closely approaching the power consumption in the power-down mode.

While burst-mode operation is possible with nearly any of today's ADCs, be sure to pay attention to the ADC data sheet and note the conditions under which the device enters the power down mode. With many ADCs, putting the device into its power down mode requires more than simply deselecting the device within a certain range of times in relation to the ADC clock.

<table>
<thead>
<tr>
<th>ADC</th>
<th>FCLK (MHz)</th>
<th>Max FS (k samples/sec)</th>
<th>Actual FS (k samples/sec)</th>
<th>Method</th>
<th>AVG Pwr (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200k samples/sec</td>
<td>1</td>
<td>50</td>
<td>10</td>
<td>Decimation</td>
<td>1,500</td>
</tr>
<tr>
<td>200k samples/sec</td>
<td>1</td>
<td>50</td>
<td>10</td>
<td>Burst</td>
<td>505</td>
</tr>
<tr>
<td>200k samples/sec</td>
<td>4</td>
<td>200</td>
<td>10</td>
<td>Burst</td>
<td>262</td>
</tr>
<tr>
<td>1M samples/sec</td>
<td>20</td>
<td>1,000</td>
<td>10</td>
<td>Burst</td>
<td>214</td>
</tr>
</tbody>
</table>

Table 1: Using decimation or burst mode operation can save considerable power in an analog to digital converter.

It is important to note that, while many ADCs are specified over a range of sample rates, these specified sample rates really relate to the range of clock rates over which these ADCs will function to specification. The sample rate achieved by these products can actually get as close to zero as desired if they support burst-mode operation, which causes the average power consumption of the ADC to approach the power consumption of the device in the power-down mode.

It becomes clear, then, that choosing an ADC with the lowest power in the power-down mode can be more important than choosing one with lowest power in the active mode. To absolutely minimize power consumption, it is necessary to consider the time in each mode and calculate the average power consumption.