Suppressing interference in adaptive-cable-equalizer designs

James Mears - May 12, 2005

Adaptive cable equalizers have seen wide use for many years in SDV (serial-digital-video) broadcasting equipment and serial telecommunications systems. Today, these same equalizers are finding increased use in other types of wired communications systems. Equalizers connect directly to coaxial or twisted-pair transmission lines and compensate for the unavoidable signal amplitude and bandwidth loss within the cables (Figure 1).

The location of an equalizer at the cable interface and its operating characteristics make it vulnerable to the effects of ESD (electrostatic discharge), EMI/RFI (electromagnetic interference/radio-frequency interference), and device-generated noise. Designing for interference suppression increases overall circuit robustness and preserves the desirable operational characteristics of these equalizers, including wide dynamic range and bandwidth, high input return loss, maximum equalized cable length, and low-noise performance.

ESD, EMI/RFI, and device-generated noise are the triple threats for wired communications systems. Moreover, ESD can damage or destroy active and passive devices, both inside and outside the circuit. CDEs (cable-discharge events) are similar to ESD but involve lower voltages. EMI/RFI can compromise system performance, often to such a degree that the system fails in its primary mission. Although device-generated noise does not usually cause system fatalities, it can degrade performance by compromising circuit operation and data integrity.

Understanding adaptive cable equalizers is the first step in dealing with interference-suppression design challenges. Designers should appreciate that adaptive cable equalizers are not simple digital devices. Whether for high- or standard-definition TV or ITU-T G.703 telecommunications, equalizers are high-performance analog devices with high gain, wide bandwidth, RF sections, and AGC (automatic-gain-control) amplifier/filters. It’s vital to remember that an analog signal carries the encoded "digital" information over the transmission line; there is no avoiding this electronic reality. The equalizer’s design enables it to handle the widely varying signal conditions of the cable interface. To minimize the effects to the equalizer by the triple threats, the system enclosure, the passive components you use with the equalizer, and the pc-board design must incorporate suitable suppression design techniques.
The gain-frequency plot in Figure 2 shows the maximum equalization response of an equalizer such as National Semiconductor's CLC014. Normally, equalizer gain and bandwidth reach a maximum when the cable that connects to the equalizer input is the maximum length that can be equalized, meaning that the signal is a minimum. But maximum gain and bandwidth also occur when the input does not connect to a cable and there is no apparent signal. Even small amounts of unwanted EMI or conducted interference, when amplified by the equalizer under these maximum-gain conditions, can compromise proper equalizer operation. However, good enclosure and pc-board design prevents interference and stops some common equalizer application faults (Table 1).

Start by guarding against ESD events

ESD events are major causes of damage to semiconductors, which are most vulnerable when conductive packaging and shipping materials do not protect them. However, they are also vulnerable after engineers have mounted them on the pc board. Although transmission-line-interface devices, such as line drivers and receivers, have high ESD-withstand-voltage ratings, good design practice recognizes that, no matter how high the ESD rating of a semiconductor, it is unwise to depend on this characteristic to provide all of the necessary ESD protection.

The design of the external circuits, and the pc board and the choice of passive components can significantly increase the protection of the driver or receiver devices. Equalizer input circuits have the added advantage of a low-impedance path through the termination network to circuit ground (Figure 2), which helps thwart ESD events. Components in the input circuit should handle the design requirements for a maximum-ESD event, unaided by other circuitry or techniques. High-voltage-rated surface-mount resistors are available from OhmCraft and other manufacturers.

Also realize that the type, mounting design, and construction of the input connector itself can complicate or ease the job of ESD suppression. Coaxial-cable connectors generally have good shielding characteristics because the outer metallic, cylindrical sleeve (shield) extends beyond the inner contact and insulator. A metallic body that is securely anchored to a conductive enclosure provides a high degree of ESD protection, because the path that the current takes in an ESD event shunts directly to the enclosure and to the safety ground, and the high voltage does not reach the pc board.

However, insulated outer bodies surround the outer conductive sleeve of other types of coaxial connectors. The sleeve terminates at the pc board with a wire lead. Therefore, in an ESD event, the path the current takes to ground through the pc board and then to the enclosure ground is longer and more resistive. In this case, the current path has more opportunity to damage the input components of the equalizer circuit.

Twisted-pair cable connectors are generally available in both shielded and unshielded versions. It is preferable to use shielded connectors even when the cable is unshielded twisted pair.

A CDE is similar to an ESD event but originates from charge stored on the cable. The charge accumulates by conductive coupling, electromagnetic coupling, or both. This charge storage is a problem mainly with unshielded twisted-pair cables. The voltage that such an event generates can reach 500V or more for any category of unshielded, twisted-pair cable. Using drain wires or shielding can reduce this voltage to 16V or less. Coaxial cables, which are shielded by their design, generally are not subject to high-voltage-discharge events. Precautions you take to suppress ESD are also effective for suppressing CDEs.

Placing transient- or ESD-suppression devices at the network input may adversely affect the return loss of the equalizer-coupling network. Depending on the location of these devices in the network,
the shunt capacitance they introduce adds lowpass filtering and affects the high-frequency impedance. Be especially careful in selecting and applying these devices, because this process may require added effort in design of the input network to maintain a high return-loss figure.

**PC-board design considerations**

Adaptive cable equalizers, with their high gain and wide bandwidth, require multilayer pc boards with separate transmission-line and power and ground layers. It is almost impossible to achieve the necessary isolation, shielding, and ESD protection using only double-sided pc boards. The power and ground layers also absorb and dissipate the energy from ESD events. The following tried and tested recommendations and techniques provide the maximum of robustness for all types of circuits.

Design power- and ground-layer pairs, or sandwiches, with 6-mil or thinner dielectrics to increase power-distribution system capacitance. This added capacitance is effective for high-frequency power-supply bypassing. Distributed capacitance values of 100 pF/in.$^2$ ($15.7 \text{ pF/cm}^2$) or more are possible with conventional pc-board dielectric materials with sandwich thicknesses of 10 mils (0.25 mm) or less. The approach increases the effective attenuation of the power-supply decoupling by 20 dB or more, and, as an added benefit, this capacitance is free.

Minimize inductance of connections to power and ground planes whenever possible. Use two vias for pad-to-plane connections of bypass capacitors, termination resistors, collector-load resistors, and $V_{CC}$ and $V_{EE}$ pins of the equalizers. Dual vias reduce interconnect inductance by as much as 50% and extend the effective operating frequency range of the bypass capacitors. Also, individually connect each $V_{CC}$ or $V_{EE}$ pin to the power or ground planes with separate vias. Do not connect multiple power and ground pins to a single via, because doing so may induce noise in the device.

Figure 3 and the corresponding pc-board layout of Figure 4 for a CLC014-based equalizer circuit illustrate critical points with several steps you can take to isolate the equalizer circuit from unwanted conducted interference. First, eliminate the noise-coupling path from the power planes to the input and AEC (adaptive-equalization-capacitor) circuits by removing the copper-plane layer under the input networks and the AEC capacitor. Doing so reduces the parasitic capacitance between the component mounting pads, the component bodies, and the planes. Parasitic capacitance can couple device-generated and power-supply noise into the equalizer inputs and the AEC-feedback loop.

Remove strips of copper (dark shaded lines in Figure 4) in all planes to isolate the equalizer circuit. These "moats" almost totally surround the equalizer circuitry. The isolation forms an "analog island" for the equalizer circuit. The moats prevent signals in adjacent circuits from directly reaching the equalizer circuit through the planes. The long path between the adjacent circuits and the equalizer adds lowpass filtering and attenuates unwanted signals.

Designers frequently place cable drivers adjacent to the equalizer to provide a signal-loop-back function. The cable-driver output-signals are usually larger than the signal that the equalizer receives. The relatively large-amplitude output signal can couple into the equalizer input, causing data corruption or unwanted output signals. Moats prevent the cable-drive signal from interfering with the equalizer inputs.

Reduce the effects of RFI pickup by enclosing the input in a well-grounded guard (shield) ring. This ring should completely enclose the equalizer input circuits and connect to all ground-plane layers at several points. You can use copper floods instead of guard rings on the outer pc-board layers (Figure 5). To be an effective shield, these floods must connect to all ground planes at intervals of about 1 cm.
To reject RFI, use a symmetrical input-component layout. Doing so maximizes the common-mode cancellation that the differential inputs of the equalizer provide. RFI is a common-mode signal if both inputs receive it equally. A symmetrical input-circuit layout with balanced termination impedances tends to equalize RFI signals reaching both inputs. The common-mode rejection of the input differential amplifier cancels most of the interference signal.

Achieving good equalizer operation and minimizing interference are compatible and desirable goals (see sidebar "Design practices essential to interference-free equalizer operation"). Equalizer circuits using the interference-prevention techniques perform better and experience fewer electromagnetic and ESD upsets than circuits not using them. Adopting these techniques does not increase the cost of the design, improves product performance, and reduces the possibility of redesigns to fix equalizer interference and performance problems. Threat resistance and reliability are more economical to design in upfront than to add after a failure. (See references 1 to 11 for additional analysis and practical information.)

References