Assessing individual components is the foremost step in system thermal analysis. A component's reported thermal-resistance data becomes the gauge for thermal evaluation and management. It is therefore necessary that component manufacturers follow a known, consistent standard in providing thermal data and that they accurately characterize the data.

The JEDEC (www.jedec.org) thermal-testing standards are the most widely used in the industry today. To ensure that test methods and results are meeting JEDEC requirements, it is essential to use the proper equipment and to understand the details associated with measurement.

**Controlling junction temperatures**

Years of laboratory and real-world experience show that the life of a processing device approximately doubles for each 10°C reduction in its junction temperature. A US government study attributes more than half of electronic failures to temperature issues—more than twice the breakdown rate from vibration or humidity. Thus, the main mission for thermal management has been to keep the junction temperature of a device below its maximum allowable limit.

To achieve the goal of controlled junction temperatures, engineers have used a variety of approaches. Typically, they have combined such features as low cost, low profile, light weight, nonconductivity, and easy assembly. Their own in-house testing has typically proven their efforts to be successful.

But engineers need to ask which thermal standards, if any, were used to assess a component's thermal characteristics, and whether these tests were performed correctly. The answers to these questions, however, may be uncertain or incomplete, and lead the engineers to a broader question of whether the industry should adopt a consistent thermal-measurement methodology, such as the one that the JEDEC 51 standards provide. In the semiconductor sector, the answer is yes, and it has been since the early days of the JEDEC 51 series in the mid-1990s.

**JEDEC thermal standards**

JEDEC was formed in 1960 as the Joint Electron Device Engineering Council, and the industry knows it today as the JEDEC Solid State Technology Association. JEDEC is the semiconductor-engineering standardization body of the EIA (Electronic Industries Alliance), a group representing the entire electronics industry.

The group developed the JEDEC 51 standards to create a uniform method for characterizing IC packages. The standards provide a benchmark for comparing the performances of different
packages that house similar devices, or similar packages that contain different devices. You can
duplicate the results of properly performed JEDEC 51 tests and rely on them for finding effective
thermal-management solutions.

Today, 11 standards comprise the JEDEC 51 methodology for the thermal measurement of
component packages (single semiconductor device). They cover different environmental and test-
board conditions for common package types, such as wire-bond chips, leaded surface-mount
components, and perimeter and area-array through-hole leaded packages (Table 1).

The standards include very specific test parameters:

- JESD 51-2 is the natural-convection standard, requiring that a box cover the test enclosure if room
temperatures shift more than 3°C. It provides a measurement of junction to ambient thermal
resistance ($R_{\theta JA}$) that you can use as a comparison with the results of cooling methods.
- JESD 51-6 is a forced-convection test performed in a wind tunnel with uniform airflow. You take
$R_{\theta JA}$ measurements at 1m/sec and 2m/sec air speeds to measure the cooling effects of controlled
convection on a device under test.
- JESD 51-8 is the junction-to-board environmental standard that provides $R_{\theta JB}$ data under defined
conditions, including the use of cold plates to draw heat laterally into the board, and setting gap
lengths to separate the package from the cold plate and insulation. It also stipulates the
temperature range of the cooling fluid at -5 to +2°C.

Because thermal problems can lead to electronic failure, reliable JEDEC-standard thermal data can
offer a significant safeguard against recalls or field repairs. A chipmaker or board manufacturer that
tests to JEDEC 51 can provide customers with junction-temperature values for wide-ranging
applications and a variety of packaging designs. With professional testing (by a thermal lab with full
JEDEC capabilities), customers get a trustworthy and independent data source. Knowing how the die
behaves thermally means testing fewer parts and more readily finding effective cooling remedies.

The JEDEC thermal standards allow different methods for measuring junction temperatures. You can
take data using a specifically designed thermal die that is independent of the device under test or
use a dependent active die. In the active-die setup, you switch power on to raise heat to thermal
equilibrium, and then off for immediate measurement of the junction temperature. When you
perform this test using short transitions between heating and sensing, you can measure the junction
temperature, $T_J$, before the die cools significantly (Figure 1). Whether you use an independent or
active test die, you must carefully calibrate the thermal-test die, typically using a dielectric,
 Isothermal bath.

**Lab equipment for JEDEC testing**

The JEDEC 51 standards are generally easy to understand but can be challenging to set up and
perform properly. Figure 2 depicts some of the key equipment you typically use in measuring to the
standards.

Automating the testing process requires a control center. One such system is GovernerCenter,
control software for National Instruments’ LabView that the company developed to manage the
automation with different equipment for testing. A high-precision wind-tunnel controller facilitates
the air testing for wind-tunnel tests. The system achieves die calibration by automatically controlling
the isothermal-temperature bath. GovernerCenter can control all tests performed using an active die
(the recommended procedure).
**Arranging JEDEC 51-test services**

Component thermal data is some of the most important information that a manufacturer needs to provide to the electronics community. To attain accurate and timely data, JEDEC-approved equipment or a certified test lab is a valuable resource. A qualified thermal lab can test multiple boards in strict compliance with these standards while using advanced sensing and control capabilities. Because statistical significance mandates the testing of at least five components, the ability to test multiple boards in a fully automated test facility can reduce costs and provide accurate, unbiased data that is more useful to the marketplace. A qualified lab or an in-house-testing facility can provide JEDEC 51 thermal data. In either case, automation, testing accuracy, and technical know-how in the measurement process form the essential aspects of thermal-resistance data to make available as reference information.