The "need for speed" is still the driving force in all digital products. This has forced us into the transition from wide, "slow," parallel busses to narrow, fast, serial links.

Virtually all of today's high-speed serial links are differential signals with bit rates above 1 Gbps, where interconnect losses, discontinuities, intra-pair skew, and channel to channel cross talk can often limit performance. Due to design, materials, and the realities of manufacturing variations, it's not enough to just model interconnects to evaluate suitability—they must be measured and their performance compared against a compliance spec.

Of the many new high-speed serial link standards, PCI Express (formerly called 3GIO) and usually abbreviated PCI-e, has become a standard for digital communications, especially in graphics applications. Nearly all high-end graphics cards used in personal computers today have a PCI-e interface and other, outside the box applications are coming to market.

The "Gen 1" PCI-e spec is for a 2.5-Gbps channel, with the possibility of 1 to 32 channels or lanes in parallel. The second generation PCI-e specification is for a native data rate of 5 Gbps.

All single-level high-speed serial links that are formatted as non return to zero (NRZ) encode two bits of information in each clock cycle. The underlying clock frequency is half the data rate, which is called the Nyquist frequency. In a PCI-e Gen 1 signal, the bit rate is 2.5 Gbps, and the Nyquist frequency is 1.25 GHz. Since PCI-e is also encoded as 8b/10b data, the lowest repeat frequency of a bit pattern is one-tenth the bit rate, or 250 MHz.

For PCI-e Gen 1 signals, the frequency band of interest is therefore from 250 MHz to 1.25 GHz. For PCI-e Gen 2 signals with a data rate twice this, the frequency band of interest is from 500 MHz to 2.5 GHz.

The differential insertion loss specification for PCI-e compliant channels usually refers to the behavior of the interconnect in this frequency range. As a rough rule of thumb, the bandwidth of the measurement system should be at least twice the bandwidth of the frequency range of interest. In the case of PCI-e Gen 2 signals, this suggests a measurement bandwidth of at least 5 GHz.

**S-parameter measurements in serial data applications**

Fundamentally, the simplest way to characterize the behavior of an interconnect is to send precision signals into it and look at how the interconnect affects them. If the interconnect has two ends, or ports, labeled as port 1 and port 2, only two things can happen.
A signal can enter port 1, and it can be reflected back out port 1 or it can be transmitted and come out port 2. The impact of how the interconnect "scatters" the incident signal to the two ports is described by the scattering, or S-Parameters.

The parameter S11 refers to the signal that reflects back out of port 1, while S21 refers to the signal that enters on port 1 and comes out the other end at port 2. For historical reasons, the reflected signal, S11, is also called the return loss, and the transmitted signal, S21, is called the insertion loss.

In today's high speed serial links, virtually all interconnects are differential pairs, and signals are differential signals. The important properties of the interconnects are revealed in how differential signals enter port 1 and come out on either port. For analysis of differential high-speed serial networks, all measurements are done as differential, and the terms differential return loss and differential insertion loss are used.

As part of the formalism to describe differential S-parameters, the differential return loss is noted as SDD11 and the differential insertion loss is written as SDD21. The DD refers to the fact that a differential signal goes into port 1, and it is only the differential component of the response that is included in the term.

The most important metric which describes the performance of a high speed serial link is the differential insertion-loss term, SDD21. S-parameter measurements in serial data are really about measuring the SDD21 of interconnects to evaluate interconnect performance, one metric of which is how well it meets the specification.

For PCI-e Gen 1 products, the specification for SDD21 is no worse than -13.2 dB loss at the Nyquist frequency of 1.25 GHz. This is the entire loss budget, including the connectors, card wiring, and cables. With Gen 2 operating at twice the bit rate, the maximum total channel loss, SDD21, at the higher Nyquist frequency of 2.5 GHz, is the same.

Performing these measurements and evaluating how the interconnect performance compares with the loss budget at 1.25 GHz and 2.5 GHz is the core of compliance testing. Evaluating the frequency dependence of SDD21 from the low end of 250 MHz to the high end at around 5 GHz is the core of interconnect characterization.

**Measuring SDD21**

While most compliance standards are based on a frequency-domain metric, this doesn't mean the measurement has to be performed in the frequency domain. Whether measured in the time or frequency domain, the interconnect performance can be transformed and displayed in either the time domain or the frequency domain.

The frequency domain instrument is the vector network analyzer (VNA). The time-domain instrument is the time domain reflectometer (TDR). Though in principle the information content from a VNA and TDR are the same, there are a few fundamental differences in the instruments that affect the quality of the data and the ease of obtaining the required SDNA measurements.

A VNA has sophisticated and complex synthesized sources, mixers, non-linear detectors, relays, and switches in the transmission and receiver path. These elements enable the VNA to have very good frequency resolution, variable power output, and high sensitivity and dynamic range, and to automatically switch the single source they typically employ back and forth between a measurement from port 1 or from port 2.

However, the cost of this sophistication is that out-of-the-box the measurement results from a VNA
are not very accurate. The very first step is a delicate calibration process that, for a 4-port VNA, requires 18 different connections and measurements to the instrument's ports. Each has to be performed correctly and in the correct order.

A TDR, on the other hand, has a relatively controlled impedance path from the internal pulse generator to the front SMA connector. Under typical conditions, no calibration is necessary to obtain good, first-order measurements from a TDR. Turn it on, let it warm up, and it is ready to take measurements. With a simplified calibration procedure, a TDR's accuracy can be well suited for the requirements of serial data network analysis.

Rarely is a standard digital interface used with some form of coaxial connector, which could be directly connected to a VNA or TDR. Rather, multipin connectors are used, which can include 32 or more channels. To interface between the connector and the TDR, a custom circuit board is typically used. It is designed and fabricated with simple, uniform interconnects that fan-in from an array of SMA connectors at one end to the custom connector at the other end. These geometry transformer cards are referred to as fixture cards.
shows an example of a pair of fixture cards connecting a 7-m long PCI-e cable.

A measurement has in it the series combination of the device under test (DUT)—the cable in this case—and the fixture card’s SMA launch, circuit board traces, and fan-in to the connector. The total differential insertion loss of just the path on the fixture card can be as large as -1 dB at 2.5 GHz and can vary from trace to trace and board to board by as much as 20% or +/- 0.2 dB. A simplified calibration process can be used to remove the impact of the fixture card from a system measurement.

**Simplified calibration procedure for S-parameter measurements**

Because the signal path in a TDR is a very clean 50-ohm impedance per channel, a simplified calibration procedure can be used to extract just the DUT and compensate for the fixture board.

To take advantage of this process, it is important to have a reference trace on one of the boards that
corresponds to the total path traveled over the two boards, including the SMA launch on each end of the fixture boards. Since this path length is twice the length on either board, it is commonly referred to as the "2x reference thru" trace. A measurement of the 2x reference thru trace is used to compensate the system measurement to obtain just the cable DUT.

If the traces which fan into the connector are single-ended, then the 2x ref trace can be single-ended as well. If the fan-in traces utilize tight coupling, then the 2x reference traces should match as closely as possible the line widths and couplings of the actual fan-in traces. In the fixture board of the fan-in traces are uncoupled and the 2x reference line is single-ended.
The first step in a TDR-based S-parameter measurement is to measure the time domain transmitted response of the 2x reference trace with the two channels of the TDR, the positive channel and the negative channel. Conceptually speaking, the ratio between these two measurements is the time-domain differential insertion loss of all the interconnects from the TDR pulse source—the connectors and the cables to the fixture board, the SMA launches, and the traces on the board. An example of the measured time domain transmitted responses is shown in
The second step is to measure the differential transmitted response of the complete system composed of the fixture board and cable assembly. A positive and negative stimulus must be applied to the DUT. These can be recorded as separate waveforms and then processed in software to obtain the differential transmitted response, or they can be subtracted directly on the TDR instrument so only the one differential transmitted response needs to be recorded.

This simplifies the process to perform an S-parameter measurement of a channel to basically two measurements, the differential transmitted signal through the 2x reference thru, and the differential transmitted signal through the system assembly. An example of these two measurements is shown in
Turning these time-domain differential transmitted signals into SDD21 displays is all done in software with one mouse click. The resulting differential insertion loss response from this time domain measurement is shown in

In this example of a 0.5-m PCI-e cable, the differential insertion loss at 1.25 GHz is -1.3 dB, while at 2.5 GHz it is -2.0 dB. These values are well
within the acceptance spec of the PCI-e Gen 1 and Gen 2 requirements of no worse than -7.5 dB for the cable alone. Of course, the cable is just one element of the complete interconnect path, so these values would be used in a loss budget analysis for the entire link.

It is also of interest to measure the actual contribution from the losses in the fixture board. To measure this requires first measuring the insertion loss of the TDR source and receiver and the cables from the TDR to the 2x reference trace. This measurement is used as a reference to the time domain insertion loss of the 2x reference trace.
It is interesting to note that the attenuation from just the FR4 in the roughly 0.1 m of total trace length on the fixture board has about half the loss of the 0.5-m cable assembly that is to be measured. If the fixture contribution was not compensated, the insertion loss of the DUT would have been measured as about 50% larger than it really was.

Since the losses associated with the fixture board can be a significant fraction of the DUT losses, variations in the differential insertion loss of the traces from the SMA launch to the connector to the DUT will act as uncontrolled random variations in every DUT measurement.

An implicit assumption in this compensation method is that the losses in the 2x reference trace match the combined losses of the two traces on the two fixture boards, with their SMA launches. Even if the 2x reference thru is designed to match the line widths and lengths of the fan-in traces, the natural variations from fabricating two different boards and the local changes in glass weave and resin variations can give more than 20% variation in the differential insertion loss between actual traces. This corresponds to about 0.2-dB variation at 2.5 GHz, from just the trace to trace variation. This natural uncertainty arising from the use of economical, circuit-board-based geometry transformers, is well above the typically 0.05-dB intrinsic noise floor in a TDNA measurement.
As a final comparison, the differential insertion loss of a 7 meter long cable assembly was measured and compared with the 0.5 m cable. The results are shown in
Below about 6 GHz, the longer cable shows about 5x higher attenuation than the short cable. In addition to the attenuation, some of the losses arise from the connector impedance mismatch and coupling losses, which cause reflections that are proportionally higher in the short cable relative to the insertion loss.

The striking feature in the measured differential insertion loss is the sharp drop off at about 8 GHz. This is probably due to a time-delay skew between the two lines that make up the differential pair measured. For a dip at 8 GHz, the time-delay skew would have to be about 60 psec between the two lines in the differential pair. If this were all due to a length difference, and none due to local
dielectric constant variation, the length skew needed to account for this dip is 13 mm, out of the total cable length of 7 m, or about 0.2%.

Of course, this does not contribute to cable performance near the PCI-e Gen 2 Nyquist frequency of 2.5 GHz, but does illustrate the role of real-world manufacturing issues in interconnect performance, and why accurate, routine, and simple measurements are important to verify compliance.

Beyond compliance testing

There is a wealth of information in the differential insertion-loss measurements in addition to whether or not it meets a compliance test, or the value of the loss to be used in a loss budget analysis.
propagation through the interconnect. With a synthesized pseudo random bit sequence (PRBS), and the measured insertion loss, the effective eye diagram from this interconnect can be simulated.

![Eye Diagram](image)

An example of a 5-Gbps eye for this 7-m-long cable. This shows the eye diagram mask test, with and without equalization, as specified by the PCI Express standard.

TDR-based S-parameter measurements of an interconnect are key ingredients to evaluate the interconnect’s performance for high-speed serial-link applications. This often means comparing its performance to a compliance spec, or to obtain a loss value for a loss budget, or even to explore the potential margin for a next-generation application. Real-world variations in product requires a measurement of an interconnect to evaluate its performance. The simpler and easier a measurement is, the more it is likely to be used when needed.

Time-domain S-parameter measurements takes advantage of the controlled impedance interconnect
path inherent in a TDR instrument to enable a simplified measurement and calibration process for
differential insertion loss of any interconnect. With an inherent noise floor well below the natural
variation in the fixture performance, its accuracy is well suited for serial data network
measurements and its ease of use dramatically lowers the barriers to routine applications.