It would be a masterpiece of understatement to suggest that control loop compensation holds much significance in power converter design. This is true in part because of increasing demand for ultra-fast load transient dynamic response—especially with voltage regulator modules (VRMs) targeted at the VCORE applications (Reference 1)—and in part because of concerns for loop stability and its direct implications for product robustness and reliability. It is also true that the burgeoning popularity, perceived advantages and abundant methods of current mode control (CMC), including peak, valley, average and emulated inductor current techniques (Reference 2) or hybrid schemes like enhanced $V^2$ control (Reference 3), have diverted focus from traditional voltage mode control (VMC) as the loop control methodology prevalent in DC-DC power conversion. This may have emanated from the conventional wisdom that when compensating voltage mode converters, more design choices are necessary and significant a priori knowledge and design know-how are required to extract an optimum design.

The theme of this article seeks to examine the particulars of voltage mode control as applied to output voltage regulation in buck or buck-derived converter topologies. First and foremost, the power and control stages are reviewed with respect to the small-signal model and relevant transfer functions. It is demonstrated how the crossover frequency of the loop gain is significant in the context of the frequency range where feedback is effective in attenuating the closed-loop characteristics, such as output impedance and audio susceptibility. Control loop compensation is described with heuristic analysis and design procedure. It is revealed that the multiple design iterations and somewhat complicated component selection procedures hitherto proposed and commonly employed with voltage mode compensation analysis and design can be simplified to the extent that, from a user perspective, the essence of single-loop voltage mode control can be considered relatively straightforward and intuitive vis-à-vis multiloop current mode control.

More particularly, the merits and demerits of fully integrated, partially integrated and fully external compensation components are distilled in the context of ease of design and flexibility with IC type PWM controllers and regulators. To this end, specific examples of practical implementations with monolithic CMOS regulator ICs as well as a BiCMOS controller IC based solution, all from National Semiconductor, are underscored to conclude the discussion.
Buck converter power and control stage review

The generalized schematic of a single phase/channel synchronous buck converter using voltage mode control and a type III compensation circuit is embodied in

Non-ideal power train components are shown in the foregoing schematic with parasitics such as inductor DC resistance, $R_{DCR}$, and capacitor equivalent series resistance, $R_{ESR}$, denoted explicitly. Second order parasitics, such as capacitor equivalent series inductance (ESL) and interconnection impedances, are not represented. The high side switch is driven by a PWM signal for time $t_{on}$ in each switching period of duration $T_s$. The duty cycle ratio $D$ is given by
The low side switch is driven complementarily with duty cycle \( D' = 1 - D \). Both switches operate at fixed switching frequency \( f_s = 1/T_s \). The output filter consists of inductor \( L_o \) and capacitor \( C_o \). For simplicity, the driver and deadtime generation stage with associated logic are denoted in block format.

A conventional op-amp type voltage error amplifier represents the epicenter of the control loop structure. The divided down output voltage at the error amplifier inverting input, usually termed the feedback (FB) node, is compared to a fixed reference voltage, \( V_{ref} \), and a compensated error signal is generated at the compensation node, labeled COMP. This error signal is compared to a saw-tooth ramp voltage at the pulse width modulator (PWM) comparator such that an increase in COMP leads to a commensurate increase in duty cycle command for the power stage. Trailing-edge modulation is underlined herein whereby a turn-on command is activated at the clock edge and a turn-off command is imposed when COMP intersects the ramp voltage. Alternative PWM strategies chronicled in the technical literature include leading-edge and double-edge modulation.

Buck converter small-signal analysis

The appropriate small-signal average model (Reference 4) for the single- (and multi-) phase buck converter circuit is manifested in
Using standard averaging and linearization techniques around a DC operating point, the small-signal duty cycle perturbation, designated $\hat{d}(s)$ in the Laplace domain, effectuates a resultant linear variation in output voltage, $\hat{v}_{\text{out}}(s)$. Four small-signal functions of the loaded power converter system are of salient importance:

- open-loop gain;
- PID compensator transfer function;
- closed-loop line-to-output transfer function;
- closed-loop output impedance.

These parameters are easily derived from the small-signal model and are given respectively by equations 2 to 5, where $C_o$ is the output capacitance value (appropriately derated for applied voltage and operating temperature), $R_L$ is the effective load resistance and $R_{\text{DAMP}}$ is the total series damping resistance associated with the inductor DCR, power FET $R_{\text{DS(ON)}}$ and PCB trace resistance.

Although the loop gain is of primary importance, a regulator is not specified directly by its loop gain, but by its performance related characteristics, namely closed-loop output impedance and line-to-output transfer function.

$$G_{\text{vd}}(s) = \left. \frac{\hat{v}_{\text{out}}(s)}{\hat{d}(s)} \right|_{\hat{v}_{\text{in}}(s)=0, \hat{i}_{\text{out}}(s)=0}$$

$$= \frac{v_{\text{in}}}{(R_L + R_{\text{DAMP}})^{\frac{1}{2}} + sL_o + sC_o + s^2L_oC_o}$$

These equations provide a comprehensive understanding of the system's behavior under small-signal perturbations.
The open-loop control-to-output voltage transfer function in the Laplace domain is given by equation 2, or more succinctly in its normalized form by

\[
Z_o(s) = \frac{\hat{v}_{\text{out}}(s)}{\hat{i}_{\text{out}}(s)} \bigg|_{\dot{v}(s)=0} \, \hat{v}_{\text{in}}(s)=0
= \frac{R_{\text{ESR}} + \frac{1}{sC_o}}{(R_{\text{DAMP}} + sL_o)(1 + sR_{\text{ESR}}C_o)} R_L
= \frac{R_L R_{\text{DAMP}} (1 + sL_o/R_{\text{DAMP}})(1 + sR_{\text{ESR}}C_o)}{(R_L + R_{\text{DAMP}}) + s[L_o + C_o(R_{\text{ESR}}(R_L + R_{\text{DAMP}}) + R_L R_{\text{DAMP}})] + s^2L_oC_o(R_L + R_{\text{ESR}})}
\]

\[
G_{vg}(s) = \frac{\hat{v}_{\text{out}}(s)}{\hat{v}_{\text{in}}(s)} \bigg|_{\dot{v}(s)=0} \, \hat{i}_{\text{out}}(s)=0
= D \frac{R_L (1 + sR_{\text{ESR}}C_o)}{(R_L + R_{\text{DAMP}}) + s[L_o + C_o(R_{\text{ESR}}(R_L + R_{\text{DAMP}}) + R_L R_{\text{DAMP}})] + s^2L_oC_o(R_L + R_{\text{ESR}})}
\]

\[
G_c(s) = \frac{\hat{v}_{\text{comp}}(s)}{\hat{v}_{\text{out}}(s)} = \frac{(1 + sR_{C1}C_C)\left[1 + s\left(R_{\text{FB1}} + R_{C2}\right)C_C\right]}{sR_{\text{FB1}}C_C\left[1 + sR_{C1}C_C\right]} \frac{C_{C2}}{C_C + C_{C2}}
\]

Open loop transfer function

The open-loop control-to-output voltage transfer function in the Laplace domain is given by equation 2, or more succinctly in its normalized form by

\[
G_{vd}(s) \equiv V_{\text{in}} \frac{1 + \frac{s}{\omega_{\text{ESR}}}}{1 + \frac{s}{Q_o\omega_o} + \frac{s^2}{\omega_o^2}}
\]

Evidently, the power stage transfer function of a voltage mode buck converter has a complex double pole related to the LC output filter and a left half plane zero due to the output capacitor ESR, the locations of which are given respectively by

\[
f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{L_oC_o\left[1 + \frac{R_{\text{ESR}}}{R_L}\right]}} \approx \frac{1}{2\pi\sqrt{L_oC_o}}
\]
\[
f_{ESR} = \frac{\omega_{ESR}}{2\pi} = \frac{1}{2\pi R_{ESR} C_O}
\]  

Equation (8)

\(f_c\) and \(f_{ESR}\) represent the LC filter complex double pole and output capacitor ESR zero, respectively.

The PWM modulator gain, \(F_M\), is inversely proportional to the peak-to-peak ramp voltage, and given by

\[
F_M = \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = \frac{1}{V_{ramp}}
\]  

Equation (9)

Error amplifier finite gain-bandwidth notwithstanding, the compensator transfer function from output voltage to COMP node given by equation 5 can be more aptly written as

\[
G_C(s) \equiv K_{midband} \frac{\left(1 + \frac{\omega_{z1}}{s}\right) \left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)}
\]  

Equation (10)

The type III compensator produces three poles and two zeros. One pole is located at the origin to realize high DC gain while the frequencies of other singularities—signified by red (pole) and blue (zero) dashed rings surrounding the relevant components in
values as follows

\[
\omega_{z1} = \frac{1}{R_{C1}C_{C1}}; \quad \omega_{z2} = \frac{1}{(R_{FB1} + R_{C2})C_{C3}}
\]
\[
\omega_{p1} = \frac{1}{R_{C2}C_{C3}}; \quad \omega_{p2} = \frac{1}{R_{C1}(C_{C1}||C_{C2})} \approx \frac{1}{R_{C1}C_{C2}}
\]  \hspace{1cm} (12)

The open-loop transfer function of the system, denoted by \( T_v(s) \) in
\[
\hat{v}_{\text{out}}(s) = G_{vd}(s) \hat{d}(s) + G_{ig}(s) \hat{v}_{\text{in}}(s) - Z_o(s) \hat{i}_{\text{out}}(s)
\]

measured by breaking the loop, injecting a variable frequency oscillator signal and recording the ensuing frequency response using a gain-phase analyzer setup, is given by

\[
T_v(s) = \frac{\hat{v}_{\text{comp}}(s)}{\hat{v}_{\text{out}}(s)} \frac{\hat{v}_{\text{out}}(s)}{\hat{d}(s)} \frac{\hat{d}(s)}{\hat{v}_{\text{comp}}(s)} = G_c(s) G_{vd}(s) F_M
\]  

(13)
shows a bode plot of the loop gain and phase of a typical system. The poles and zeros of the system are marked with × and o symbols respectively, and a + symbol indicates the bandwidth at crossover.
typify the individual gain and phase characteristics of the LC filter, modulator and compensator.

**Output impedance**

The open-loop output impedance in the Laplace domain, \( Z_o(s) \), is the parallel LCR impedance looking back into the output filter and load given by [equation 3](#), or more succinctly in its normalized form by

\[
Z_o(s) \equiv \frac{R_{DAMP} \left(1 + \frac{s}{\omega_L}\right) \left(1 + \frac{s}{\omega_{ESR}}\right)}{1 + \frac{s}{Q_o \omega_o} + \frac{s^2}{\omega_o^2}} = \frac{G_{vd}(s)}{V_{in}} Z_L(s) \quad (14)
\]
Here, it is assumed that the duty cycle perturbation $\dot{d}(s)$ is zero with no feedback control. The parameter $\omega_L = L_o/R_{DAMP}$ is the inductor zero frequency and $Z_L(s) = R_{DAMP} + sL_o$. The open-loop output impedance is limited by the parasitic resistance $R_{DAMP}$ at low frequency and the output capacitor at high frequency. The closed-loop output impedance can be derived from the small-signal block diagram in

$$\hat{v}_{out}(s) = G_{vl}(s)\dot{d}(s) + G_{vg}(s)\hat{v}_{in}(s) - Z_o(s)i_{out}(s)$$

and corresponds to the open-loop impedance divided by the feedback factor $[1 + T_v(s)]$, i.e.
This coincides with the usual properties of single-loop feedback systems. The importance of the loop gain is now apparent and the relationship between loop gain and closed-loop parameters is generally intuitive in single-loop systems. Consider the case where a current $I_{out}$ represents the nominal load current and $i_{out}$ is a source of perturbation. If $i_{out}$ is a step function, the corresponding $\hat{v}_{out}$ is the system step response governed by $Z_{oCL}(s)$. Thus, $Z_{oCL}(s)$ provides an assessment of the output voltage response to a load current transient demand.

$$Z_{oCL}(s) = -\left. \frac{\hat{v}_{out}(s)}{\hat{i}_{out}(s)} \right|_{\hat{v}_{in}(s)=0} = \frac{Z_o(s)}{1 + T_v(s)}$$  \hspace{1cm} (15)
Two salient points are noteworthy: (a) the output impedance of the regulator should be much less than the load impedance and (b) the effective "bandwidth" of the output impedance should be much larger than the bandwidth of the load to achieve fast recovery from load transients.

illustrates the open- and closed-loop output impedance of a typical system. The difference between the open- and closed-loop responses is effectively the loop gain and the two plots converge within 3dB of each other at the loop gain crossover frequency, denoted by the + symbol in
Note that no additional attenuation is achieved at higher frequencies by closed-loop feedback.

**Line disturbance rejection**

The open-loop line-to-output transfer function—also termed power supply ripple rejection (PSRR) or audio susceptibility—is defined as the transfer function from perturbation of the input voltage to perturbation of the output voltage with duty ratio held constant. This transfer function, $G_{vg}(s)$, given in the Laplace domain by equation 4 contains the same poles and zeros as $G_{vd}(s)$ and can thus be written in its normalized form as

$$G_{vg}(s) \equiv D \frac{1 + s}{\omega_{ESR}} + s^2 \frac{1}{Q_o \omega_o + s \omega_o^2} = \frac{G_{vd}(s)}{V_{in}} D$$

(16)

Again, it is assumed the duty ratio D is fixed with no AC variation, i.e. no feedback control. The closed loop line-to-output transfer function can be obtained (in similar fashion to the aforementioned closed loop output impedance) as

$$G_{vg\text{ CL}}(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)|_{\hat{i}_{out}(s)=0}} = \frac{G_{vg}(s)}{1 + \hat{T}_v(s)}$$

(17)
By evaluating the loop gain and making it as large as possible and with high bandwidth, the open-loop audio susceptibility can be largely attenuated by closed-loop operation right up to the bandwidth of the loop gain.

shows the open- and closed-loop audio susceptibility characteristics of a typical system. The closed-loop parameter has particular significance in terms of line regulation when a 100/120-Hz signal is superimposed on the converter input or when the input to a point-of-load buck converter (POL) is connected to the output of an unregulated intermediate bus converter (IBC) as part of a distributed power architecture.
Buck converter VMC compensation design

The conventional compensation strategy (References 5 and 8) employed with voltage mode control is to use two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero and one compensator pole located at one half switching frequency to attenuate high frequency noise.

- $f_{z1} = f_{z2} \leq f_o$;
- $f_{p1} = f_{ESR}$;
- $f_{p2} = f_s/2$;

\[
\begin{align*}
T_v(s) &= \frac{V_{in}}{V_{ramp}} \left( \frac{1 + \frac{s}{\omega_{z1}}} {sR_{FB1}C_C1} \right) \left( \frac{1 + \frac{s}{\omega_{z2}}} {1 + \frac{s}{\omega_{p1}}} \right) \left( \frac{1 + \frac{s}{\omega_{ESR}}} {1 + \frac{s}{Q_o\omega_{LC}} + \frac{s^2}{\omega_{LC}^2}} \right) \\
T_v(s) &\approx \frac{R_{C1} \left( R_{FB1} + R_{C2} \right) C_C3}{sR_{FB1}} \frac{1}{L_OC_O} \frac{V_{in}}{V_{ramp}}
\end{align*}
\]
Essentially, a multiorder system is reduced to a single order approximation by judicious choice of compensator components.

portrays a comparison of the exact and approximate loop gains expressions presented in equation 18 and equation 19, respectively, using a typical converter circuit. Excellent correlation is obtained at low frequency and around crossover when the compensator singularities are located as described.
Regularly, the value of $R_{C2}$ is much less than $R_{FB1}$, particularly with ceramic output capacitors where the resultant ESR zero is located at high frequency. Realizing that $\| \tau_\nu(s) \|_{s=\omega_0} = 1$, a simple solution for the crossover frequency with type III voltage mode control is derived from equation 19 as

$$f_c = \frac{R_{C1}C_{C3}}{2\pi L_0 C_0} \frac{V_{in}}{V_{ramp}}$$

(20)

Knowing the desired location of the compensator poles and zeros, values for $R_{C2}$, $C_{C1}$, $C_{C2}$ and $R_{FB1}$ can be calculated from the design-oriented expressions in equation 21 based from those in equation 12, assuming an initial value is selected for $R_{C1}$. $R_{FB2}$ is then selected based on the desired output voltage.

$$C_{C1} = \frac{1}{\omega_1 R_{C1}} ; C_{C2} = \frac{1}{\omega_2 R_{C1}} ; C_{C3} = \frac{\omega_c L_0 C_0 V_{ramp}}{R_{C1} V_{in}} ;$$

$$R_{C2} = \frac{1}{\omega_2 C_{C3}} ; R_{FB1} = \frac{1}{\omega_1 C_{C3}} - R_{C2} ;$$

$$R_{FB2} = \frac{R_{FB1}}{\left( \frac{V_{out}}{V_{ref}} \right)} - 1$$

(21)

Referring again to the system bode plot in

![System Bode Plot](image-url)
the phase margin, indicated as $\Phi M$, is the difference between the loop phase and $-180^\circ$. A target of 50° to 60° for this parameter is considered ideal. Indeed, for a second order system with single-loop control, phase margin is directly related to transient response and a phase margin of 52° results in closed loop-peaking factor $Q_o$ of unity (Reference 4). More phase margin can be dialed in by locating the compensator zeros at a frequency lower than the LC double pole.

**Buck converter IC implementations**

There has been a range of CMOS buck regulator parts recently offered by semiconductor manufacturers that advantageously incorporate the power MOSFETs, driver stage and control loop section to achieve a high density power supply solution. To attain even higher density and lower component count, some or all of the control components are integrated into the IC. Generally, given a semiconductor process, a lot of work is focused on producing the smallest area circuit. Knowing that chip area comes with a premium cost, capacitive component fabrication is problematic—capacitors with a large energy storage requirement will use an excessive amount of die area. This places a limitation on the compensation capacitor value. Other key considerations when appraising a particular regulator IC implementation are as follows:

- access to the COMP node for power supply characterization, bode plot measurement, soft-start or enable functions;
- line feedforward and associated complexity;
- flexibility, ease-of-use, filter inductor and capacitor limitations;
- component count, reliability;
- component footprints, PC board real estate requirements;
- integrated compensation component initial tolerance and temperature coefficient.
illuminate examples of low voltage (2.95V to 5.5V input voltage range) CMOS buck regulator implementations from National Semiconductor (Reference 5 and 6) with fully integrated and partially compensation components, respectively.

The LM2853 has all the classic type III compensation components incorporated internally, including output voltage setpoint resistors. This creates a high density solution with low parts count and reduced pick-and-place operations during automated SMT manufacturing process. However, unlike the LM2854, the LM2853 implementation generally has no option to pursue high bandwidth closed-loop performance or optimum transient response. This stems from the realization that a conservative loop design is necessary to accommodate a broad range of output filter components.

The LM2854 has internal type II compensation components located around the error amplifier between FB and COMP. These are designed to locate a pole at the origin and a pole at half switching frequency. Furthermore, a zero is located at 8.8 kHz or 17.6 kHz for the 500 kHz or 1 MHz switching frequency options, respectively, to approximately cancel the most likely location of one LC filter pole. The three external compensation components, \( R_{FB1} \), \( R_C \) and \( C_C \), are easily selected by simple design expressions to position a zero at or below the LC pole location and a pole to cancel the ESR zero.
shows an example of a buck converter using a LM3743 BiCMOS voltage mode PWM controller IC (Reference 7). In addition to the output voltage setpoint resistors, the five components that embody type III compensation are discrete parts, usually realized with 0402 or 0603 size surface-mount passives. These components are user-defined and facilitate maximum flexibility with the control loop design and implementation. To this end, the availability of compensator design software from IC vendors can greatly assist in the compensation component selection process. The power supply designer then has all the tools at his/her disposal to optimally position the loop crossover frequency while maintaining adequate phase margin over the required power supply line, load and operating temperature ranges.

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