Capacitive touch switch uses CPLD

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Capacitive touch switches work by measuring the change in capacitance of a PCB (printed-circuit-board) pattern depending on the placement of a user’s finger over a sensing pad. Capacitive switches are becoming popular because they are less expensive than mechanical switches. Using the features of an Altera MAX IIZ CPLD (complex-programmable-logic device), you can implement a touch-switch decoder with no external components. The touch sensor employs an 8-mm-diameter sensing pad on the PCB using the solder mask as a dielectric. The circuit decodes a single switch, but you could use the approach for multiple switches, and it has programmable sensing thresholds that allow for different PCB layouts and dielectrics.

Figure 1 shows a simple circuit with no external components other than the capacitive-switch layout on the PCB. A basic touch-switch PCB layout is on the left. It comprises only an 8-mm copper circle surrounded by copper that connects to ground. The dashed line shows that the center sensor connects to the CPLD using a via and a backside copper trace. A solder mask acting as a dielectric covers the center sensor and ground. The PCB touch sensor becomes a variable capacitor, $C_{TOUCH}$. 

The variable capacitor is part of a relaxation oscillator. The CPLD has a built-in weak pullup resistor on each I/O pin. \( C_{\text{TOUCH}} \) and the weak pullup resistor create an RC circuit. If the PINOSC (pin-oscillator) signal is low, the I/O pin will be low, making the D input to the PINOSC LPM (library-o-parameterized-modules) register low. LPM blocks come from the Quartus II LPM.

The register and other logic in the circuit use a free-running, 4.4-MHz internal oscillator, ALTUFM oscillator, as a clock. On the rising edge of the clock, PINOSC goes low, making the buffer-driving pin go to a high-impedance state. The weak pullup resistor slowly makes the pin voltage rise based on an RC time constant. Not touching the switch causes it to have the lowest capacitance and fastest rise time. Touching the switch causes it to have the highest capacitance and the slowest rise time. The pin-I/O buffer uses the Schmitt-trigger option of the CPLD to reduce the noise sensitivity of the slow-rising pin signal. Once the pin node reaches the high-voltage threshold, the D input of the PINOSC registers a zero. On the next clock edge, the PINOSC signal goes low, driving the pin node low for one full clock cycle. This PINOSC circuit oscillates at two fundamental frequencies, depending on the state of the touch capacitor. Putting the register into the oscillator loop reduces noise and makes the oscillator stable and synchronous with the decoding logic. The PINOSC period is always a multiple of 1/4.4 MHz or the frequency of the internal oscillator.

The switch decoder counts the period of 16 PINOSC cycles and compares it with a known time period. If 16 or more cycles happen in less than the sample period, it means that no one is touching the switch. If fewer than 16 cycles happen in the sample period, it means that someone is touching the switch, and the PINOSC oscillation becomes slower. The lower LPM counter sets the sample period.
Figure 2 Representative waveforms that Figure 1 illustrates have a top-counter modulus of 3; a bottom-counter modulus of 12; and pin-oscillator periods of 3 and 6, respectively.

For example, the sample signal was active once every 80 clock cycles in a prototype (Figure 2). The upper LPM counter measures the period of 16 PINOSC cycles. After 16 cycles, the fast signal goes high and stays high until the sample signal resets it. The fast signal is a one in the prototype when 16 cycles occur in fewer than 80 cycles, making the fast signal a one when the sample signal is a one. When the sample signal is a one, the fast value clocks into the switch-LPM register. The switch-signal value updates every sample cycle with the current capacitive switch state. When you touch the switch, PINOSC is slow, and the fast signal remains a zero when the sample signal is a one, making the switch output zero. In the prototype design, the PINOSC period was three clock cycles when someone touched it and nine cycles when no one touched it. The switch threshold was five cycles. Therefore, the lower LPM-counter modulus was 5×16=80. You can use any value from four to eight, but four is too sensitive, and eight does not work for small fingers; hence, five is the best value. The upper LPM-counter modulus affects noise sensitivity. The larger the count, the more the circuit averages the period of oscillation. A low modulus makes the circuit more sensitive to random system noise. The five-cycle sensing point also allows margin for the ±25% variation among parts of the internal oscillator frequency.

Also see:

- Add a Schmitt-trigger function to CPLDs, FPGAs, and applications
- Stepper-motor motion controller and driver fit into a CPLD/FPGA
- Implement a stepper-motor driver in a CPLD