Pulse-width modulation is a simple way to modulate, or change, a square wave. In its basic form, the duty cycle of the square wave changes according to some input. The duty cycle is the ratio of high and low times in the square wave. A waveform with a 50% duty cycle would be high for 50% of the time and low for 50% of the time, and a waveform with a 10% duty cycle would be high for 10% and low for 90%. Many applications exist for PWM, including motor control, servo control, light dimming, switching power supplies, and even some audio amplifiers. In applications such as MEMS (micro-electromechanical-system) mirror-actuator control, a feedback system needs to regulate the PWM. A circuit monitors and controls the PWM output and varies the duty cycle according to the requirements of the application. The output frequency tunes the actuator, and the duty cycle sets the actuator's speed. The feedback loop controls the threshold level. This Design Idea describes a high-frequency, high-resolution PWM with feedback control. First, it might be useful to discuss some PWM theory.

**Alternative architectures**

Traditional PWMs use two op amps to generate a sawtooth waveform, a potentiometer to generate a dc reference, and a comparator to generate the PWM output. The advantage of this type of design is that the circuit is practical and inexpensive. Unfortunately, you cannot easily program the frequency without changing component values, and fine-frequency tuning is difficult. Another problem with this method is that accurate control of the duty cycle is difficult. You could use a digital potentiometer in place of the mechanical one, but this replacement results in a more costly design. A second method for generating PWM waveforms uses an ADµC824 MicroConverter. In addition to providing two PWM outputs, it also integrates ADCs, DACs, an 8052-compatible microcontroller, and flash memory. You can configure the PWM with resolution as high as 16 bits. However, the programmed frequency affects the resolution of the PWM. The frequency and resolution of the PWM are as follows: \[ F_{PWM} = \frac{16.777\text{ MHz}}{N} \], where \( N \) is the resolution in bits.

An internal PLL derives the 16.77-MHz reference clock from a 32-kHz crystal. This reference clock samples the output of the PWM. As stated, \( N \), the number of bits, is the resolution of the PWM. For 16-bit resolution the maximum frequency is 266 Hz. The resolution at 200 kHz drops to approximately 6 bits. Thus, the ADµC832 is the ideal low-cost approach for low-frequency, high-resolution applications but not for a high-frequency, high-resolution application.

**DDS implementation**

Applications requiring high-resolution frequency tuning and pulse-width-modulation tuning in real time can use a DDS (direct digital synthesizer) to provide a high-accuracy sawtooth waveform with
fine-frequency resolution across a large bandwidth. You can then use this signal as the input to a comparator in either open- or closed-loop applications. **Figure 1** shows an easy method of generating programmable square waves with programmable duty cycles. The AD9833 DDS drives a programmable triangular wave into one input of the AD8611 comparator and controls the frequency of the output waveform. The feedback loop from the actuator controls the threshold level of the comparator. The AD8611 is a single 4-nsec comparator with a latch function and complementary output. The input signal from the DDS connects directly to the inverting input of the comparator. The output feeds back to the noninverting input through \( R_1 \) and \( R_2 \). The ratio of \( R_1 \) to \( R_1 + R_2 \) establishes the width of the hysteresis window with \( V_{DAC} \) setting the center of the window or the average switching voltage. The output switches low when the input voltage is greater than \( V_{HI} \) and does not switch high again until the input voltage is lower than \( V_{LO} \), as the following expressions show: 

\[
V_{HI} = V^+ - 1.5 V - V_{DAC}/(R_1/(R_1 + R_2)) + V_{DAC},
\]

and 

\[
V_{LO} = V_{DAC}/(R_2/(R_1 + R_2)),
\]

where \( V^+ \) is the positive supply voltage to the comparator and \( V_{DAC} \) is the level that the DAC sets. The AD8611 can accept a 100-MHz signal with 400-mV p-p levels and can also accept input signals in the tens of millivolts. The AD9833 can provide sinusoidal- and triangular-wave outputs using the DDS architecture. It includes a numerical-controlled oscillator employing a 28-bit phase accumulator, a sine ROM, and a 10-bit D/A converter on a single chip (**Figure 2**).
You typically think of sine waves in terms of their magnitude expression: \(a(t) = \sin(vt)\). However, these waveforms are nonlinear and are difficult to generate. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit in time. Knowing that the phase of a sine wave is linear and given a reference interval (clock period), you can determine the phase rotation for that period:

\[
\text{Phases} = \omega dt; \\
\omega = \frac{\Delta \text{Phase}}{dt}; \\
f = \frac{(\Delta \text{Phase} \times f_{\text{MCLK}})}{2\pi},
\]

where \(dt\) is the reciprocal of \(f_{\text{MCLK}}\), the master clock. You can generate output frequencies using this formula, knowing the phase and master-clock frequency. The phase accumulator provides the 28-bit linear phase. The sine ROM stores the amplitude coefficients of the output sine wave in digital format. The DAC converts the sine wave to its analog domain. If you bypass the sine ROM, the part delivers triangular waveforms instead of sinusoidal waveforms. You program the device by writing to the frequency registers. The analog output from the part is then \(f_{\text{OUT}} = (f_{\text{MCLK}}/228) \times (\text{frequency-register word})\).

The DDS outputs have 28-bit resolution, so effective frequency steps on the order of 0.1 Hz are possible to a maximum of approximately 10 MHz. Two phase registers provide 12-bit phase resolution. These registers phase-shift the signal by \(P_{\text{SHIFT}} = (2\pi/4096) \times (\text{phase-register word})\). A 25-MHz crystal oscillator provides the master reference clock for the DDS. The output stage of the DDS is a voltage-output DAC with a typical swing of 0.7V p-p into an internal 200Ω resistor. Adding load resistor \(R_L\) reduces the peak-to-peak output voltage, thus allowing you to tune the peak-to-peak output of the DDS to the input range of the comparator. A filter stage generally appears on the output of the DDS. The purpose of this stage is to filter feedthrough from the reference clock, images, and higher frequencies and to bandlimit the signals under consideration.

**Figure 3** shows typical output plots from the AD8611 comparator in **Figure 1**. The input signal from
the DDS is a triangle wave set to 1 MHz. Each plot shows the PWM output for various threshold voltages. In the closed-loop circuit of Figure 1, you can tune the output of the PWM to 12-bit accuracy. You have access to many possible ways of providing pulse-width modulation; the approach depends on the application. For low-resolution applications, traditional methods using op amps and potentiometers are acceptable and inexpensive. For low-frequency, high-resolution applications, the ADµC832 provides a one-chip approach with added features for free. For high-resolution, high-frequency applications requiring fine-frequency tuning, you can combine a DDS and a comparator to generate precise, high-frequency PWM waveforms.